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Flash Memories (Electrically Erasable and Reprogrammable Non-Volatile Memories)

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FLASH
A NEW WAY TO DEAL WITH MEMORY

Computers use memory to perform several functions—backup storage, executable code storage, and data manipulation. Today, in systems where the code changes, RAM is used to serve the function of code storage for execution by the processor. RAM also serves the purpose of allowing data manipulation in the same technology. Since DRAM is volatile, mass storage or battery-backed SRAM is used to provide nonvolatility. A small amount of ROM/EPROM also provides the storage technology to start computers (direct executable and nonvolatile).

For almost 20 years, ROM/EPROM (Read Only Memory) has been used to act as code and backup storage in dedicated applications. Scratch pad applications have used a separate RAM component.

Many interesting trends are developing to cause a growing unrest with the current MOS memory solution set.

1. CPU performance has doubled every two years, and I/O (disk) has doubled every ten years, causing a growing I/O bottleneck.
2. Lightweight solid state systems are becoming desirable and feasible in the reprogrammable environment.
3. Code for dedicated applications has grown significantly, making it increasingly difficult to stabilize, especially with standards also changing. Even changing the boot code for reprogrammable systems is becoming a desirable option.
4. Semiconductor memory costs have continued to drop faster than mass storage and are now substantially closer than 5–10 years ago. Today, disk drives are $5–$6/megabyte. EPROMs are $50–$60/megabyte.

Couple these trends with a breakthrough in MOS memory technology and you have the potential for massive change in system design and performance.

The breakthrough is Flash.

Flash is the missing technology in the MOS memory solution set. It affects all the technologies, and affects them to a greater or lesser degree as cost and performance of Flash improves and system software changes.

Flash is nonvolatile, random access, and rewritable at the same density as EPROM/DRAM. It has higher reliability than DRAM (no alpha particles), and higher reliability than disk. (Flash endurance under typical use far exceeds disks 50K mean time between failures.) Flash combines backup storage, direct execution for code, and rewritability for changes. A reprogrammable system configured around Flash does not need ROM/EPROM to boot, does not need disk for mass storage, and does not need RAM for code execution storage (RAM is still used for data manipulation).

A Flash based system would have no motor, be more reliable, lighter weight, and have higher system performance than a DRAM-based system. A high end system could use optical or other mass storage for archival purposes.

CPU's have the hardware capability to use memory in a cached write fashion today, however system software and hardware is optimized around ROM/RAM/Disk. As users realize the performance, reliability and other benefits that Intel Flash technology can provide, manufacturers will redesign their systems to take advantage of this new method of dealing with memory. Tomorrow's vision is today's choice with Intel Flash memory.

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September 1989
Order Number: 296449-001

28F256
256K (32K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - **1 Second Typical Chip-Erase**
- **Quick-Pulse Programming™ Algorithm**
  - **100 µs Typical Byte-Program**
  - **4 Second Chip-Program**
- **100 Min Erase/Program Cycles (10K Min Version Avail 1H90)**
- **12.0V V_{PP} Supply**
- **High-Performance Speeds**
  - **170 ns Maximum Access Time**
- **Low Power Consumption**
  - **100 µA Maximum Standby Current**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX™ Flash-Memory Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **Compatible with JEDEC-Standard Byte-Wide EPROM Pinouts**
  - **32-Pin Cerdip**
  - **32-Lead PLCC**

(See Packaging Spec., Order # 231369)

Intel's 28F256 CMOS flash-memory offers the most cost-effective and reliable alternative for updatable non-volatile memory. The 28F256 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be erased and reprogrammed: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F256 increases memory flexibility, while contributing to time- and cost-savings. The 28F256 is targeted for alterable code- or data-storage applications where traditional E^2PROM functionality (byte-erasure) is either not required or not cost-effective. The 28F256 can also be applied where EPROM ultraviolet erasure is impractical or time-consuming.

The 28F256 is a 256-kilobit non-volatile memory organized as 32768 bytes of 8 bits. Intel's 28F256 is offered in 32-pin Cerdip or 32-lead PLCC packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Intel's 28F256 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 170 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 µA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from $-1V$ to $V_{CC} + 1V$.

With Intel's ETOX™ (EPROM tunnel oxide) process base, the 28F256 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

SAN039980

October 1989
Order Number: 290158-006

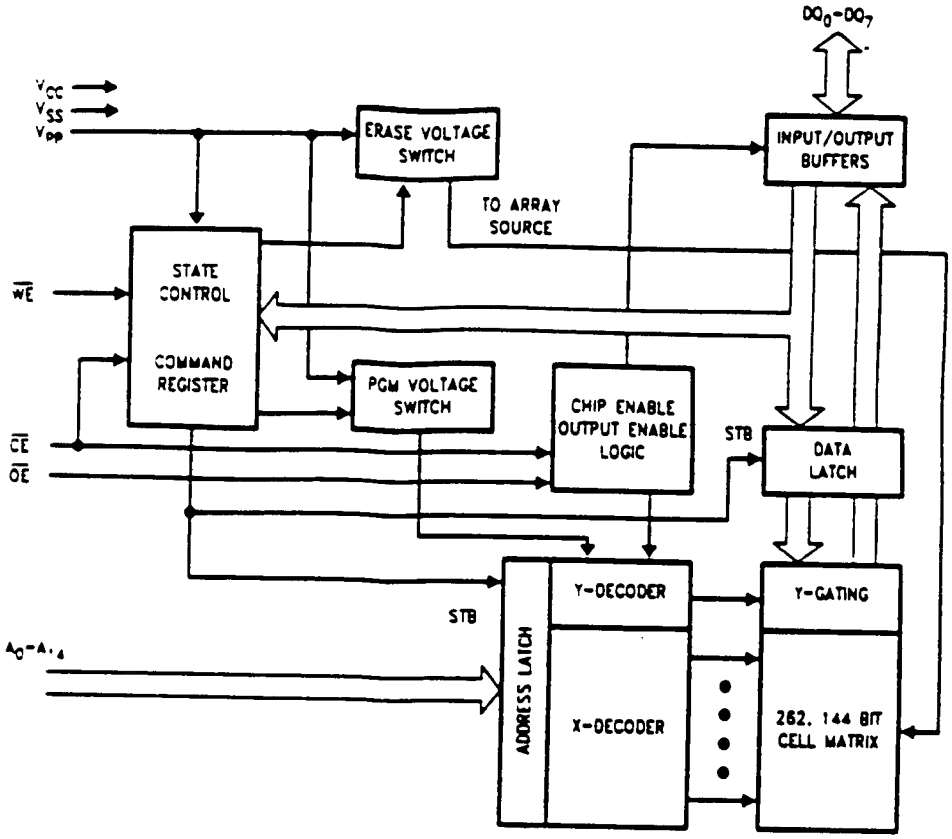

Figure 1. 28F256 Block Diagram

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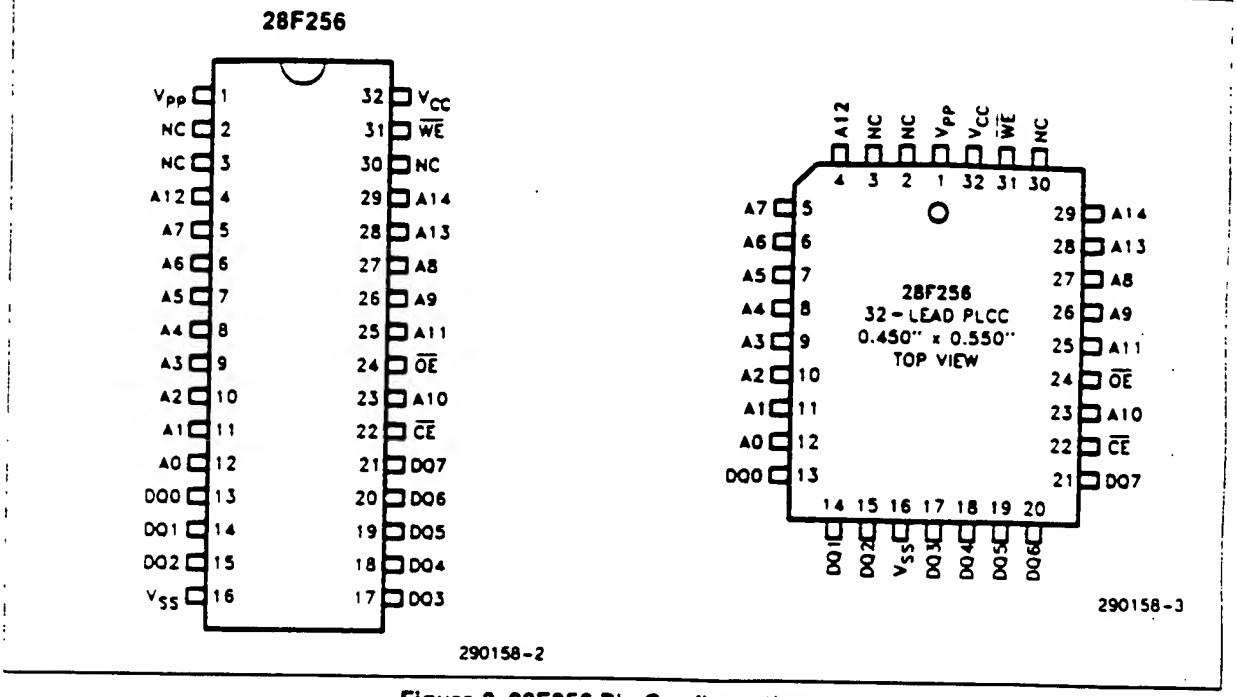

Figure 2. 28F256 Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{14}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} \leq V_{CC} - 2V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ± 10%)
V_{SS}		**GROUND**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.

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APPLICATIONS

The 28F256 flash-memory adds electrical chip-erasure and reprogrammability to EPROM non-volatility and ease of use. The 28F256 is ideal for storing code or data-tables in applications where periodic updates are required. With a minimum of 10,000 erase/program cycles available as an option, the 28F256 also serves as a dense, nonvolatile data acquisition and storage medium.

The need for code updates pervades all phases of a system's life—from prototyping to system manufacture to after-sale service. In the factory, during prototyping, revisions to control code necessitate ultraviolet erasure and reprogramming of EPROM-based prototype codes. The 28F256 replaces the 15- to 20-minute ultraviolet erasure with one-second electrical erasure. Electrical chip-erasure and reprogramming occur in the same workstation or PROM-programmer socket.

Diagnostics, performed at subassembly or final assembly stages, often require the socketing of EPROMs. Socketed test codes are ultimately replaced with EPROMs containing the final program. With electrical chip-erasure and reprogramming, the 28F256 is soldered to the circuit board. Test codes are programmed into the 28F256 as it resides on the circuit board. Ultimately, the final code can be downloaded to the device. The 28F256's in-circuit alterability eliminates unnecessary handling and less-reliable socketed connections, while adding greater test flexibility.

Material and labor costs associated with code changes increase at higher levels of system integration—the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revisions to EPROM-based code require the removal of EPROM components or entire boards. The service technician performs the twenty-minute ultraviolet erasure and reprogramming on-site, or returns boards to the factory for rework. An alternate approach is to use one-time-programmable EPROMs. The service technician removes the "old" devices and replaces them with updated versions. The used components are discarded.

Designing with the in-circuit alterable 28F256 eliminates socketed memories, reduces overall material costs, and drastically cuts the labor costs associated with code updates. With the 28F256, code updates are implemented locally via an edge-connector, or remotely over a serial communication link.

The 28F256's electrical chip-erasure, byte reprogrammability, and complete nonvolatility fit well with data accumulation needs. Electrical chip-erasure gives the designer a "blank-slate" in which to log data. Data can be periodically off-loaded for analysis—erasing the slate and repeating the cycle. Or, multiple devices can maintain a "rolling window" of accumulated data.

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 illustrates the interface between the MCS®-51 micro-

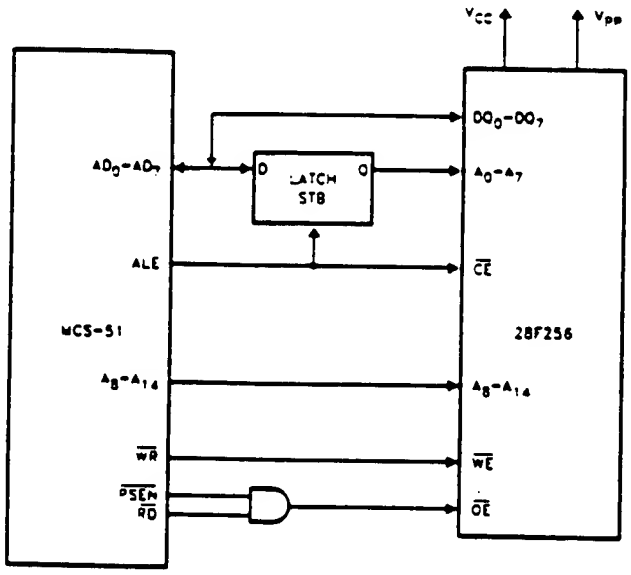

Figure 3. 28F256 in an MCS®-51 System

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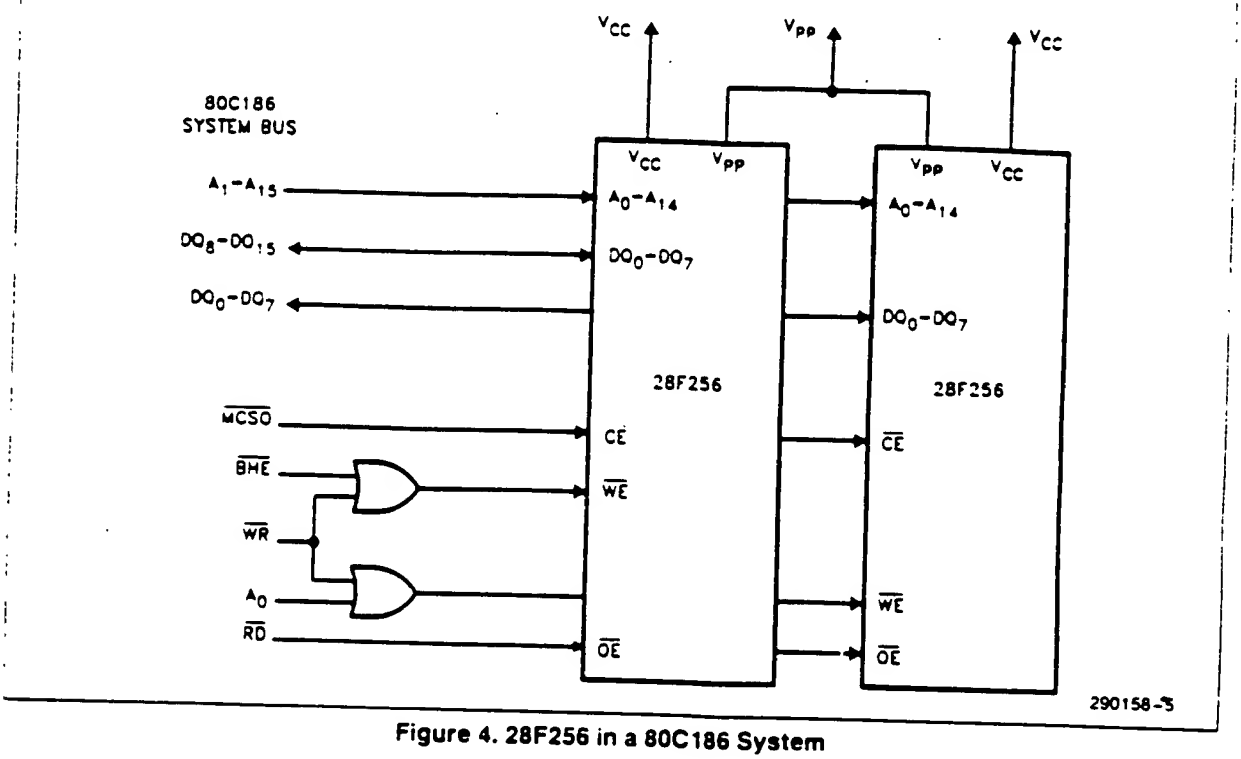

Figure 4. 28F256 in a 80C186 System

controller and one 28F256 flash-memory in a minimum chip-count system. Figure 4 depicts two 28F256s tied to the 80C186 system bus. In both instances, the 28F256's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents. (Comprehensive system design information is included in AP-316, "Using the 28F256 Flash Memory for In-System Reprogrammable Nonvolatile Storage", Order Number 292046-002).

With cost-effective in-system reprogramming and extended cycling capability, the 28F256 fills the functionality gap between traditional EPROMs and E²PROMs. EPROM-compatible specifications, straightforward interfacing, and in-circuit alterability allows designers to easily augment memory flexibility and satisfy the need for updatable nonvolatile storage in today's designs.

PRINCIPLES OF OPERATION

Flash-memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 28F256 introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 28F256 is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and int$_e$ligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—int$_e$ligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the int$_e$ligent Identifier codes, or output data for erase and program verification.

The command register is only alterable when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When high voltage is removed,

Table 2. 28F256 Bus Operations

Operation	Pins	V_{PP}(1)	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	int$_e$ligent ID™ Manufacturer(2)	V_{PPL}	V_{IL}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	int$_e$ligent ID™ Device(2)	V_{PPL}	V_{IH}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = B1H or B2H
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out(4)
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby(5)	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In(6)

NOTES:
1. V_{PPL} may be ground, a no-connect with a resistor tied to ground, or $\leq V_{CC} - 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to D.C. Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. Device code B1H requires $V_{PPH} = 12.0V \pm 5\%$. Device code B2H requires $V_{PPH} = 12.75V \pm 0.25V$. All other addresses low.
3. $11.5V \leq V_{ID} \leq 13.0V$.
4. Read operations with $V_{PP} = V_{PPH}$ may access array data or the int$_e$ligent ID™.
5. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V_{IL} or V_{IH}.

the contents of the register default to the read command, making the 28F256 a read-only memory. Memory contents cannot be altered.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this instance, all operations are performed in conjunction with the command register. The 28F256 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read

The 28F256 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Figure 7 illustrates read timing waveforms.

The read operation only accesses array data when V_{PP} is low (V_{PPL}). When V_{PP} is high (V_{PPH}), the read operation can be used to access array data, to output the int$_e$ligent Identifier™ codes, and to access data for program/erase verification.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 28F256's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. If the 28F256 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

int$_e$ligent Identifier™

The int$_e$ligent Identifier operation outputs the manufacturer code (89H) and device code (B1H). Programming equipment automatically matches the device with its proper erase and programming algorithms.

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With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage (11.5V–13.0V) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 28F256 is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B1H).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

The three high-order register bits (R7, R6, R5) encode the control functions. All other register bits, R4 to R0, must be zero. The only exception is the reset command, when FFH is written to the register. Register bits R7–R0 correspond to data inputs D7–D0.

Refer to A.C. Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 28F256 register commands.

Table 3. Command Definitions

Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
	Req'd	Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read Intelligent ID™(4)	1	Write	X	90H	Read	IA	ID
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification (Mfr = 89H, Device = B1H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
5. Figure 6 illustrates the Quick-Erase™ Algorithm.
6. Figure 5 illustrates the Quick-Pulse Programming™ Algorithm.
7. The second bus cycle must be followed by the desired command register write.

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Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the 28F256, the device powers-up and remains enabled for reads until the command-register contents are changed. Refer to the A.C. Read Characteristics and Waveforms for specific timing parameters.

inteligent Identifier™ Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not desired system-design practice.

The 28F256 contains an inteligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of B1H or B2H. To terminate the operation, it is necessary to write another valid command into the register.

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to A.C. Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 28F256 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. Figure 6, the Quick-Erase™ Algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F256. Refer to A.C. Erase Characteristics and Waveforms for specific timing parameters.

Set-up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to A.C. Program-

ming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command

The 28F256 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The 28F256 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 7, the 28F256 Quick-Pulse Programming™ Algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to A.C. Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 100 μs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 7 illustrates the Quick-Pulse Programming algorithm.

QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The 28F256 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately four seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. A total of seventy-nine erase operations are allowed. Erasure typically occurs in one second. Figure 8 illustrates the Quick-Erase Algorithm.

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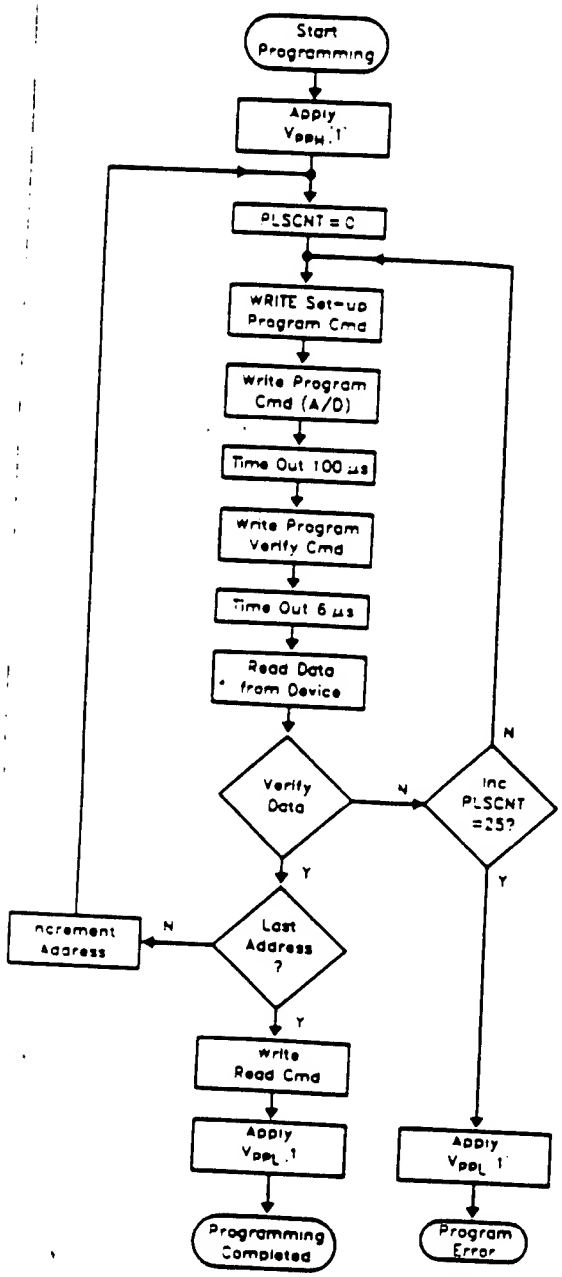

Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Addr ss/Data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H: Stops Program Operation
Standby		t_{WHGL}
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H. Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:
1. See D.C. Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or less than V_{CC} − 2.0V. Refer to Principles of Operation.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.

Figure 7. 28F256 Quick-Pulse Programming™ Algorithm

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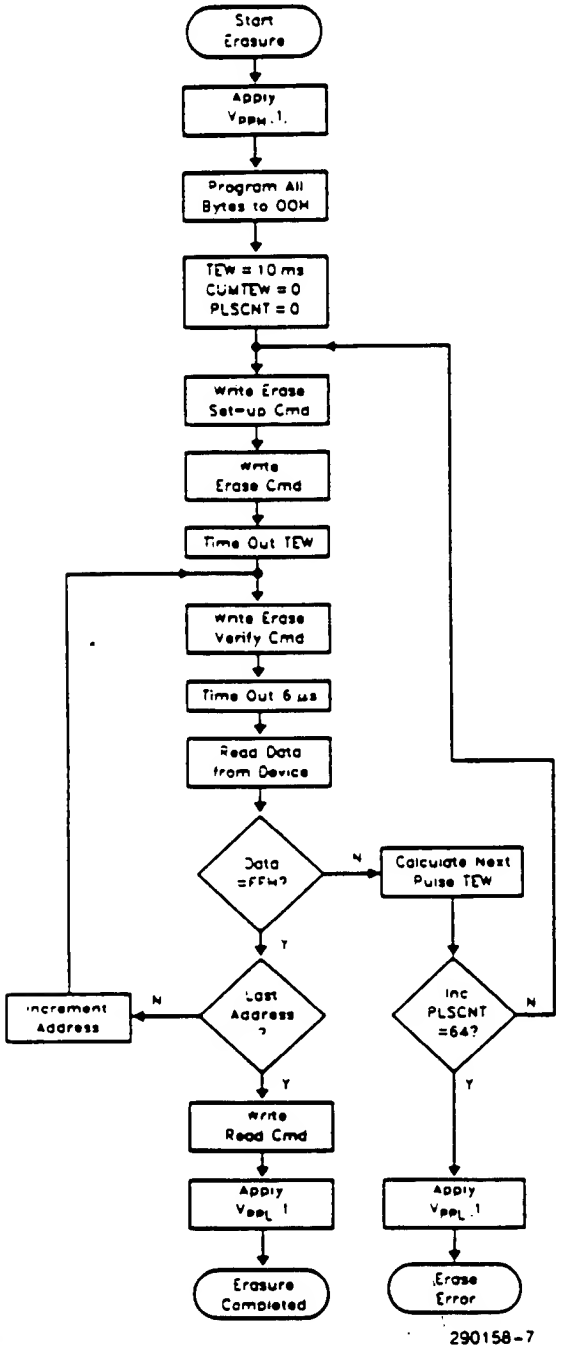

Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Use Quick-Pulse Programming™ Algorithm (Figure 5)
		Initialize: Erase Time Cum. Erase Time Pulse-Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH CUMTEW = CUMTEW + TEW TEW = Truncated Integer Divide INT(CUMTEW/8)
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:
1. See D.C. Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or less than V_{CC} + 2.0V. Refer to Principles of Operation.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.

Figure 8. 28F256 Quick-Erase™ Algorithm

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DESIGN CONSIDERATIONS

Two-Line Output Control

Flash-memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation and,
b. complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash-memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Sequencing

The 28F256 is designed to offer protection against accidental erasure or programming, caused by spurious system-level signals that may exist during power transitions. The 28F256 powers-up in its read-only state. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of the two-step command sequences. While these precautions are sufficient for most applications, it is recommended that V_{CC} reach its steady-state value before raising V_{PP} above V_{CC} − 2.0V. In addition, upon powering-down, V_{PP} should be below V_{CC} − 2.0V, before lowering V_{CC}.

Additional Information

	Order Number
AP-316, "Using the 28F256 Flash Memory for In-System Reprogrammable Nonvolatile Storage"	292046
27F256 Data Sheet	290157
ER-21 "Intel's 27F256 and 28F256 Flash Memories"	294004
ER-20 "ETOX™ Flash Memory Technology"	294005
RR-60 "ETOX™ Flash Memory Reliability Data Summary"	293002

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
- During Read ..... 0°C to +70°C(1)
- During Erase/Program ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
Voltage on Any Pin with
- Respect to Ground ..... −2.0V to +7.0V(2)

Voltage on Pin A_9 with
- Respect to Ground ..... −2.0V to −13.5V(2, 3)

V_{PP} Supply Voltage with
- Respect to Ground
- During Erase/Program .... −2.0V to +14.0V(2, 3)

V_{CC} Supply Voltage with
- Respect to Ground ..... −2.0V to +7.0V(2)

Output Short Circuit Current ..... 100 mA(4)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum D.C. input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} − 0.5V, which may overshoot to V_{CC} − 2.0V for periods less than 20 ns.
3. Maximum D.C. voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current		±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current		1.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$
I_{CC1}	V_{CC} Active Read Current		30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current		30	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current		30	mA	Erasure in Progress
I_{PPS}	V_{PP} Leakage Current		±10	µA	$V_{PP} = V_{PPL}$

SAN039992

D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
I_{PP2}	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} − 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage	2.4		V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 Intelligent Identifier™ Voltage	11.50	13.00	V	$A_9 = V_{ID}$
I_{ID}	A_9 Intelligent Identifier™ Current		500	µA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations	0.00	V_{CC} − 2.0V	V	**NOTE:** Erase/Program are inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations	11.40 12.50	12.60 13.00	V	B1H: V_{PP} = 12.0V Device B2H: V_{PP} = 12.75V Device
V_{PPDV}	V_{PPH} Difference between Erase/Program & Verify		0.20	V	B1H: V_{PP} = 12.0V Device

D.C. CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		± 1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current		± 10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current		100	µA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC}$ ± 2V
I_{CC1}	V_{CC} Active Read Current		30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current		30	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current		30	mA	Erasure in Progress
I_{PPS}	V_{PP} Leakage Current		± 10	µA	$V_{PP} = V_{PPL}$

SAN039993

D.C. CHARACTERISTICS—CMOS COMPATIBLE (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
I_{PP2}	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} − 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA, $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage	0.85 V_{CC}		V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ Min
V_{OH2}		V_{CC} − 0.4			I_{OH} = −100 µA, $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifer™ Voltage	11.50	13.00	V	$A_9 = V_{ID}$
I_{ID}	A_9 intelligent Identifier™ Current		500	µA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations	0.00	V_{CC} − 2.0V	V	**NOTE:** Erase/Programs are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations	11.40	12.60	V	V_{PP} = 12.0V
V_{PPDV}	V_{PPH} Difference between Erase/Program & Verify		0.20	V	B1H: V_{PP} = 12.0V Device

CAPACITANCE(1) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Limits		Unit	Conditions
		Min	Max		
C_{IN}	Address/Control Capacitance		6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

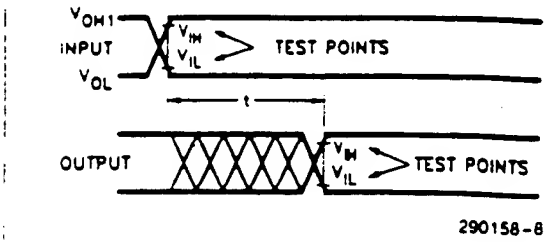
NOTE:
1. Sampled, not 100% tested.

A.C. TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... V_{OL} and V_{OH1}
Input Timing Reference Level ..... V_{IL} and V_{IH}
Output Timing Reference Level ..... V_{IL} and V_{IH}

SAN039994

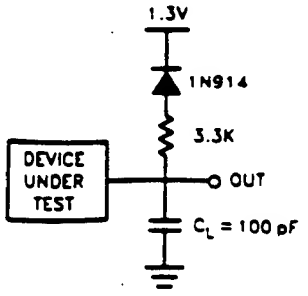
A.C. TESTING INPUT/OUTPUT WAVEFORM



290158-8

A.C Testing: Inputs are driven at V_{OH1} for a logic "1" and V_{OL} for a logic "0". Testing measurements are made at V_{IH} for a logic "1" and V_{IL} for a logic "0". Rise/Fall time ≤ 10 ns.

A.C. TESTING LOAD CIRCUIT



290158-9

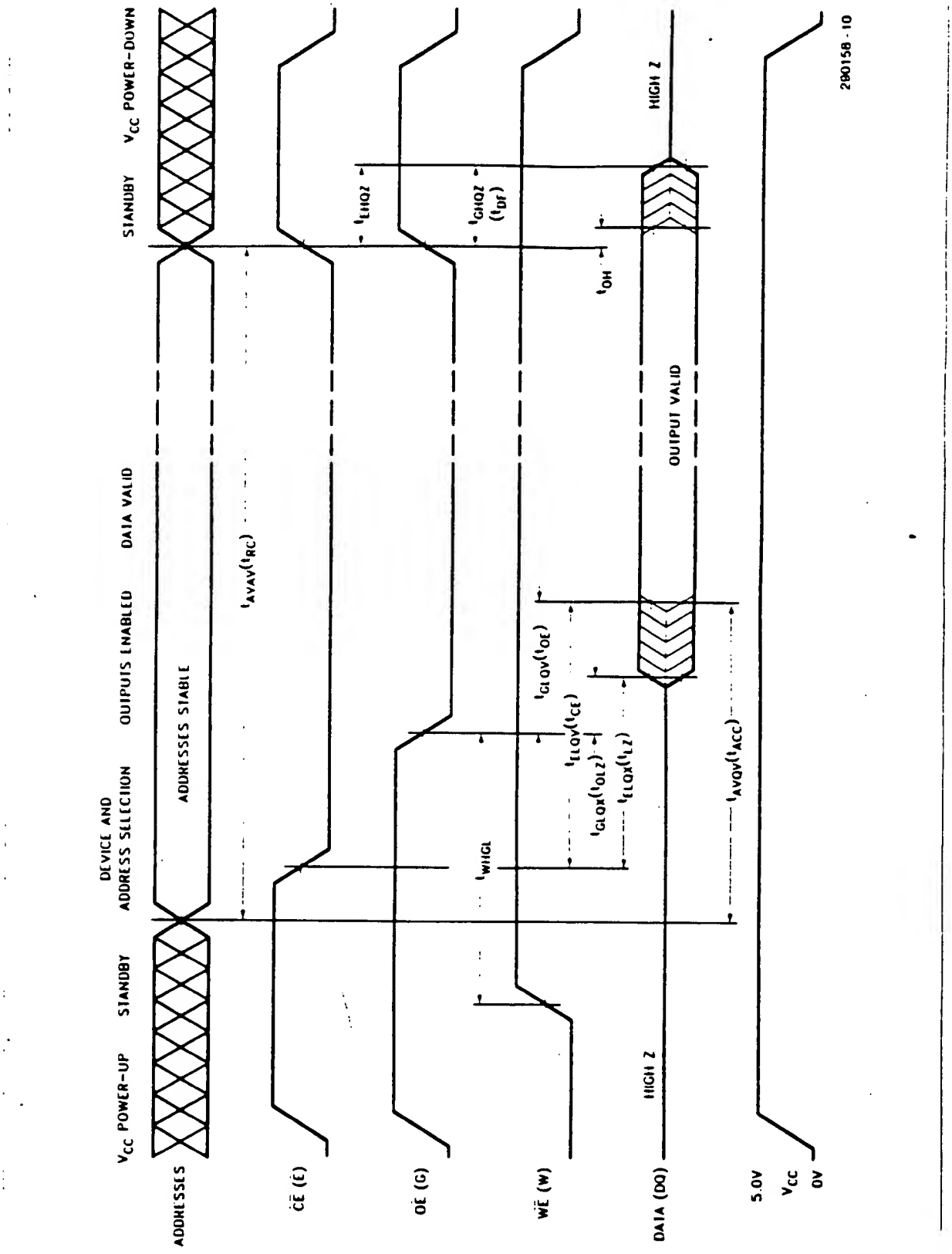
C_L = 100 pF
C_L includes Jig Capacitance

A.C. CHARACTERISTICS—Read-Only Operations

Versions		28F256-170 P1C2		28F256-200 P1C2		28F256-250 P1C2		Unit
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time	170		200		250		ns
t_{ELOV}/t_{CE}	Chip Enable Access Time		170		200		250	ns
t_{AVOV}/t_{ACC}	Address Access Time		170		200		250	ns
t_{GLOV}/t_{OE}	Output Enable Access Time		70		75		80	ns
t_{ELOX}/t_{LZ}	Chip Enable to Output in Low Z	0		0		0		ns
t_{EHQZ}	Chip Disable to Output in High Z		55		60		65	ns
t_{GLOX}/t_{OLZ}	Output Enable to Output in Low Z	0		0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z		35		45		55	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change(1)	0		0		0		ns
t_{WHGL}	Write Recovery Time before Read	6		6		6		μs

NOTES:
1. Whichever occurs first.
2. Rise/Fall Time ≤ 10 ns.

SAN039995



SAN039996

Figure 9. A.C. Waveforms for Read Operations

A.C. CHARACTERISTICS—Write/Erase/Program Operations(1)

Versions		28F256-170 P1C2		28F256-200 P1C2		28F256-250 P1C2		Unit
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time	170		200		250		ns
t_{AVWL}/t_{AS}	Address Set-Up Time	0		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time	60		75		90		ns
t_{DVWH}/t_{DS}	Data Set-up Time	50		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time	10		10		10		ns
t_{WHGL}	Write Recovery Time before Read	6		6		6		µs
t_{GHWL}	Read Recovery Time before Write	0		0		0		µs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time	20		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time	0		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width	50		60		75		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High	50		60		75		ns
t_{ELEH}	Alternate Write Pulse Width	70		80		85		ns
t_{WHWH1}	Duration of Programming Operation	95	150	95	150	95	150	µs
t_{WHWH2}	Duration of Erase Operation	(2)	(2) − 5%	(2)	(2) − 5%	(2)	(2) − 5%	
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low	100		100		100		ns

NOTES:

1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to A.C. Characteristics for Read-Only Operations.
2. The duration of each erase operation is variable and is calculated in the Quick-Erase™ Algorithm. The duration of the current erase operation is equal to the truncated value of cumulative erase time (CUMTEW) divided by eight (integer divide).

TEW = Truncated Integer Divider (CUMTEW/8)

The duration of the erase operation actually applied can exceed the calculated value by a maximum tolerance of 5%. Refer to Figure 6 for additional details.

SAN039997

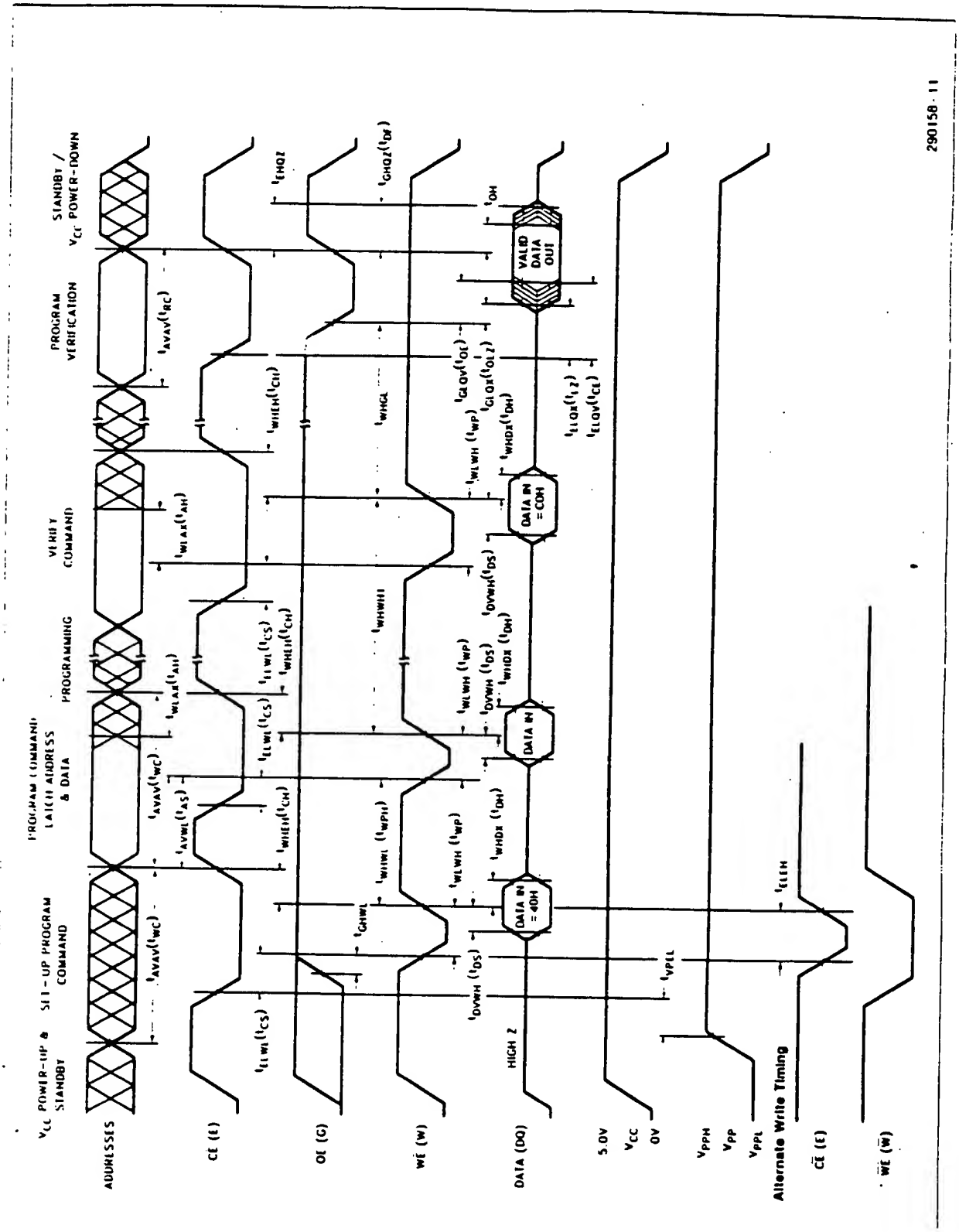
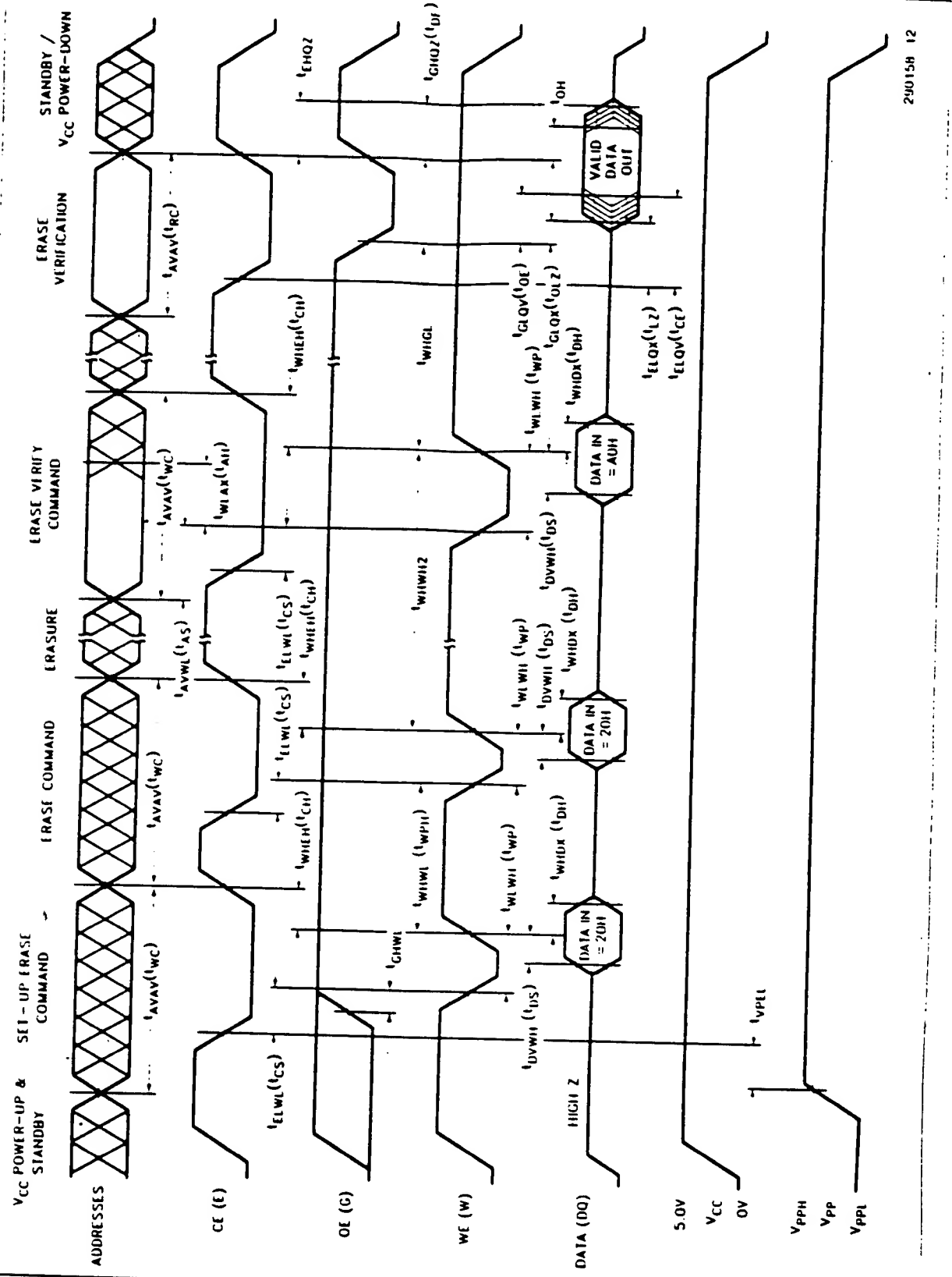


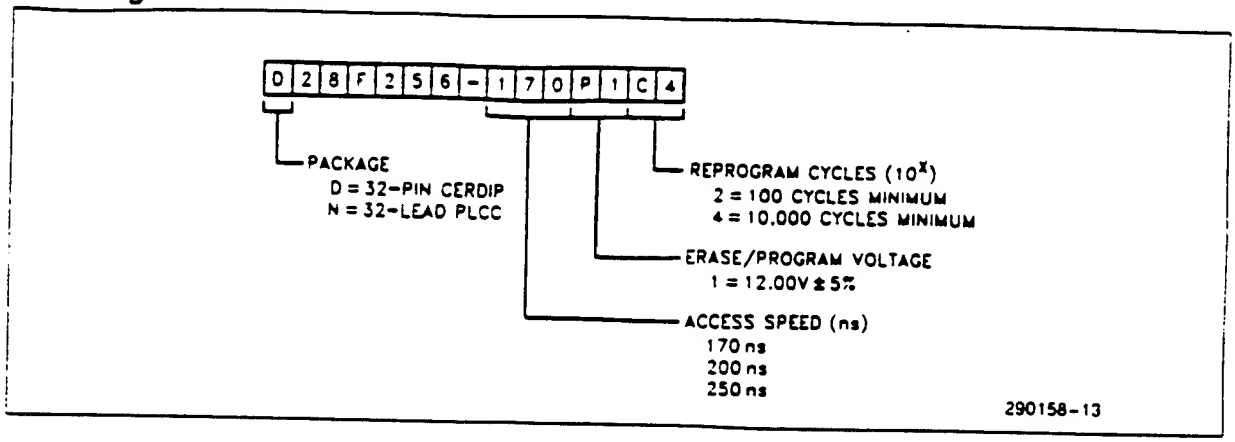
Figure 10. A.C. Waveforms for Programming Operations



SAN039999

Figure 11. A.C. Waveforms for Erase Operations

Ordering Information



VALID COMBINATIONS:

D28F256-170P1C2	N28F256-170P1C2
D28F256-200P1C2	N28F256-200P1C2
D28F256-250P1C2	N28F256-250P1C2

ADDITIONAL INFORMATION

	Order Number
AP-316, "Using the 28F256 Flash Memory for In-System Reprogrammable Non-Volatile Storage"	292046
ER-21, "Intel's 27F256 and 28F257 Flash Memories"	294004
ER-20, "ETOX™ Flash Memory Technology"	294005
RR-60, "ETOX™ Flash Memory Reliability Data Summary"	293002

SAN040000

intel

ADVANCE INFORMATION

28F256A
256K (32K x 8) CMOS FLASH MEMORY

- Flash Electrical Chip-Erase
  - 1 Second Typical Chip-Erase
- Quick-Pulse Programming™ Algorithm
  - 10 μs Typical Byte-Program
  - 0.5 Second Chip-Program
- 10,000 Erase/Program Cycles Minimum
- 12.0V ±5% V_{PP}
- High-Performance Read
  - 120 ns Maximum Access Time
- CMOS Low Power Consumption
  - 30 mA Maximum Active Current
  - 100 μA Maximum Standby Current
- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- Noise Immunity Features
  - ±10% V_{CC} Tolerance
  - Maximum Latch-Up Immunity through EPI Processing
- ETOX™-II Flash-Memory Technology
  - EPROM-Compatible Process Base
  - High-Volume Manufacturing Experience
- Compatible with JEDEC-Standard Byte-Wide EPROM Pinouts
  - 32-Pin Cerdip
  - 32-Lead PLCC

(See Packaging Spec., Order # 231369)

Intel's 28F256A CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F256A adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F256A increases memory flexibility, while contributing to time- and cost-savings.

The 28F256A is a 256-kilobit nonvolatile memory organized as 32,768 bytes of 8 bits. Intel's 28F256A is offered in 32-pin cerdip or 32-lead PLCC packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Extended erase and program cycling capability is designed into Intel's ETOX-II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F256A performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming™ and Quick-Erase™ algorithms.

Intel's 28F256A employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 120 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 μA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from −1V to V_{CC} + 1V.

With Intel's ETOX-II process base, the 28F256A levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

SAN040001

September 1989
Order Number: 290243-001

28F512
512K (64K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - **1 Second Typical Chip-Erase**
- **Quick-Pulse Programming™ Algorithm**
  - **10 µs Typical Byte-Program**
  - **1 Second Chip-Program**
- **10,000 Erase/Program Cycle Minimum**
- **12.0V ±5% V_{PP}**
- **High-Performance Read**
  - **120 ns Maximum Access Time**
- **CMOS Low Power Consumption**
  - **30 mA Maximum Active Current**
  - **100 µA Maximum Standby Current**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX™-II Flash-Memory Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **Compatible with JEDEC-Standard Byte-Wide EPROM Pinouts**
  - **32-Pin Cerdip**
  - **32-Lead PLCC**

(See Packaging Spec., Order #231369)

Intel's 28F512 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F512 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F512 increases memory flexibility, while contributing to time- and cost-savings.

The 28F512 is a 512-kilobit nonvolatile memory organized as 65,536 bytes of 8 bits. Intel's 28F512 is offered in 32-pin cerdip or 32-lead PLCC packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Extended erase and program cycling capability is designed into Intel's ETOX-II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F512 performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming™ and Quick-Erase™ algorithms.

Intel's 28F512 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 120 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 µA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from $-1V$ to $V_{CC} + 1V$.

With Intel's ETOX-II process base, the 28F512 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

SAN040002

October 1989
Order Number: 290204-003

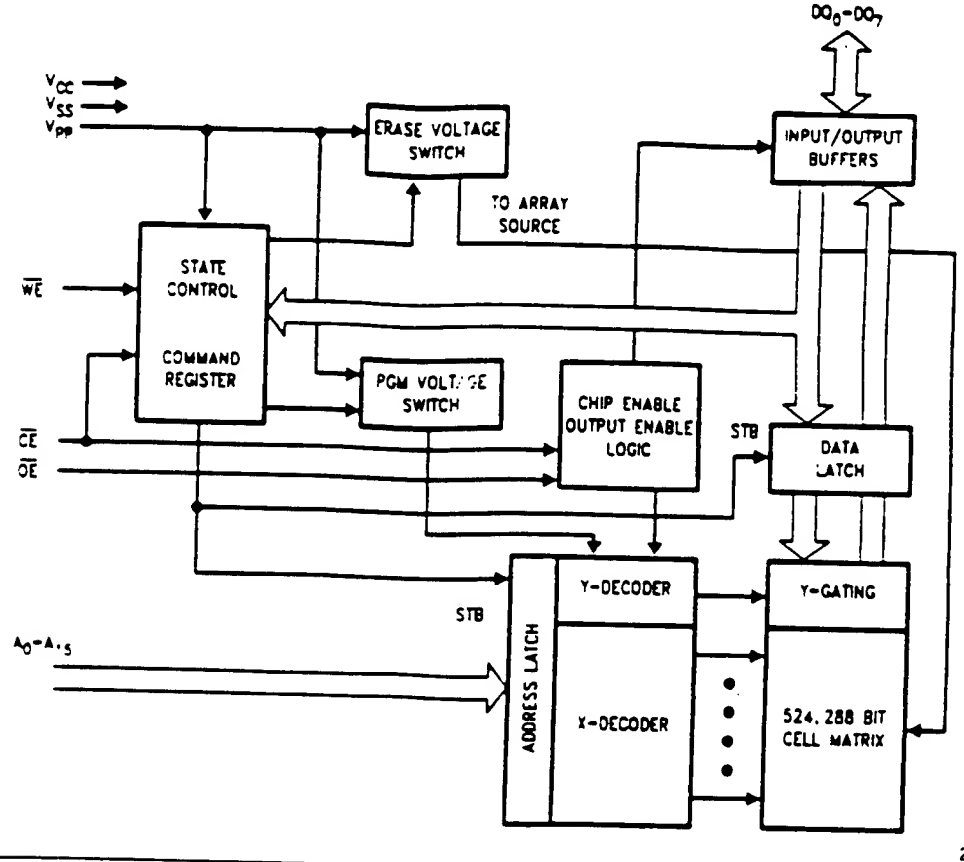


Figure 1. 28F512 Block Diagram

SAN040003

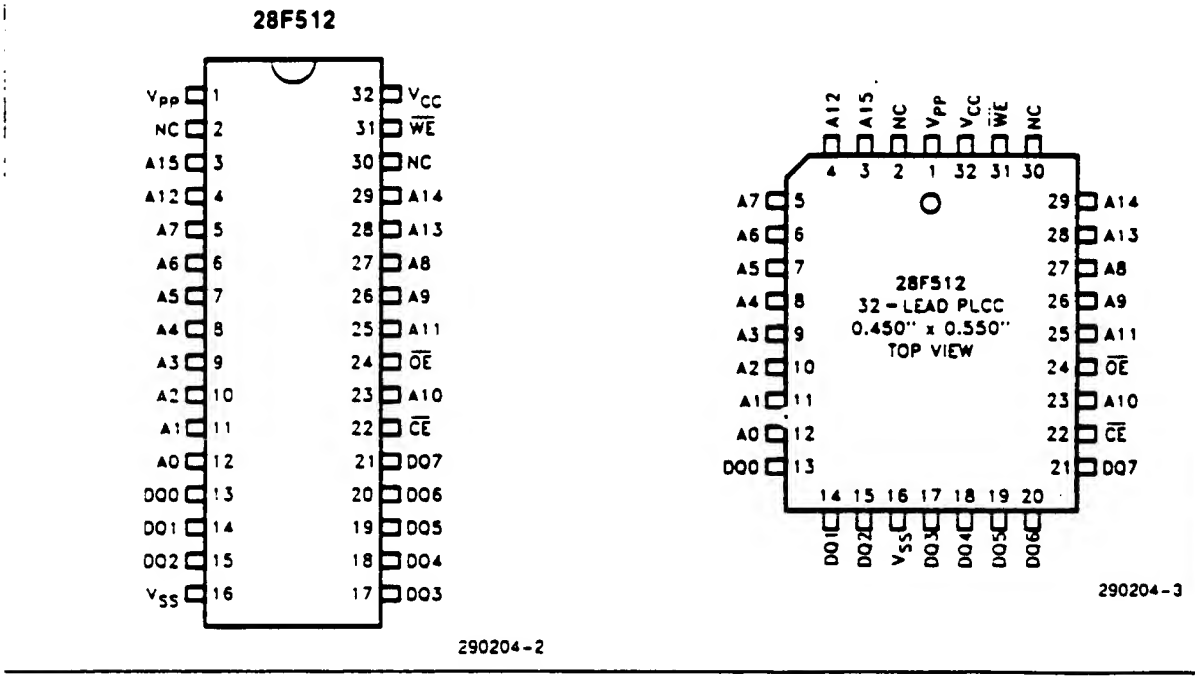


Figure 2. 28F512 Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{15}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} \leq V_{CC} - 2V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ± 10%)
V_{SS}		**GROUND**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.

SAN040004

APPLICATIONS

The 28F512 flash-memory adds electrical chip-erasure and reprogrammability to EPROM non-volatility and ease of use. The 28F512 is ideal for storing code or data-tables in applications where periodic updates are required. With a minimum of 10,000 erase/program cycles the 28F512 also serves as a dense, nonvolatile data acquisition and storage medium.

The need for code updates pervades all phases of a system's life—from prototyping to system manufacture to after-sale service. In the factory, during prototyping, revisions to control code necessitate ultraviolet erasure and reprogramming of EPROM-based prototype codes. The 28F512 replaces the 15- to 20-minute ultraviolet erasure with one-second electrical erasure. Electrical chip-erasure and reprogramming occur in the same workstation or PROM-programmer socket.

Diagnostics, performed at subassembly or final assembly stages, often require the socketing of EPROMs. Socketed test codes are ultimately replaced with EPROMs containing the final program. With electrical chip-erasure and reprogramming, the 28F512 is soldered to the circuit board. Test codes are programmed into the 28F512 as it resides on the circuit board. Ultimately, the final code can be downloaded to the device. The 28F512's in-circuit alterability eliminates unnecessary handling and less-reliable socketed connections, while adding greater test flexibility.

Material and labor costs associated with code changes increase at higher levels of system integration—the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revisions to EPROM-based code require the removal of EPROM components or entire boards. The service technician performs the twenty-minute ultraviolet erasure and reprogramming on-site, or returns boards to the factory for rework. An alternate approach is to use one-time-programmable EPROMs. The service technician removes the "old" devices and replaces them with updated versions. The used components are discarded.

Designing with the in-circuit alterable 28F512 eliminates socketed memories, reduces overall material costs, and drastically cuts the labor costs associated with code updates. With the 28F512, code updates are implemented locally via an edge-connector, or remotely over a serial communication link.

The 28F512's electrical chip-erasure, byte reprogrammability, and complete nonvolatility fit well with data accumulation needs. Electrical chip-erasure gives the designer a "blank-slate" in which to log data. Data can be periodically off-loaded for analysis—erasing the slate and repeating the cycle. Or, multiple devices can maintain a "rolling window" of accumulated data.

With high density, nonvolatility, and extended cycling capability, the 28F512 offers an innovative alternative for mass storage.

Integrating main memory and backup storage functions into directly executable flash memory boosts system performance, shrinks system size, and cuts power consumption. Reliability exceeds that of electromechanical media, with greater durability in extreme environmental conditions.

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 depicts two 28F512s tied to the 80C186 system bus. The 28F512's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

SAN040005

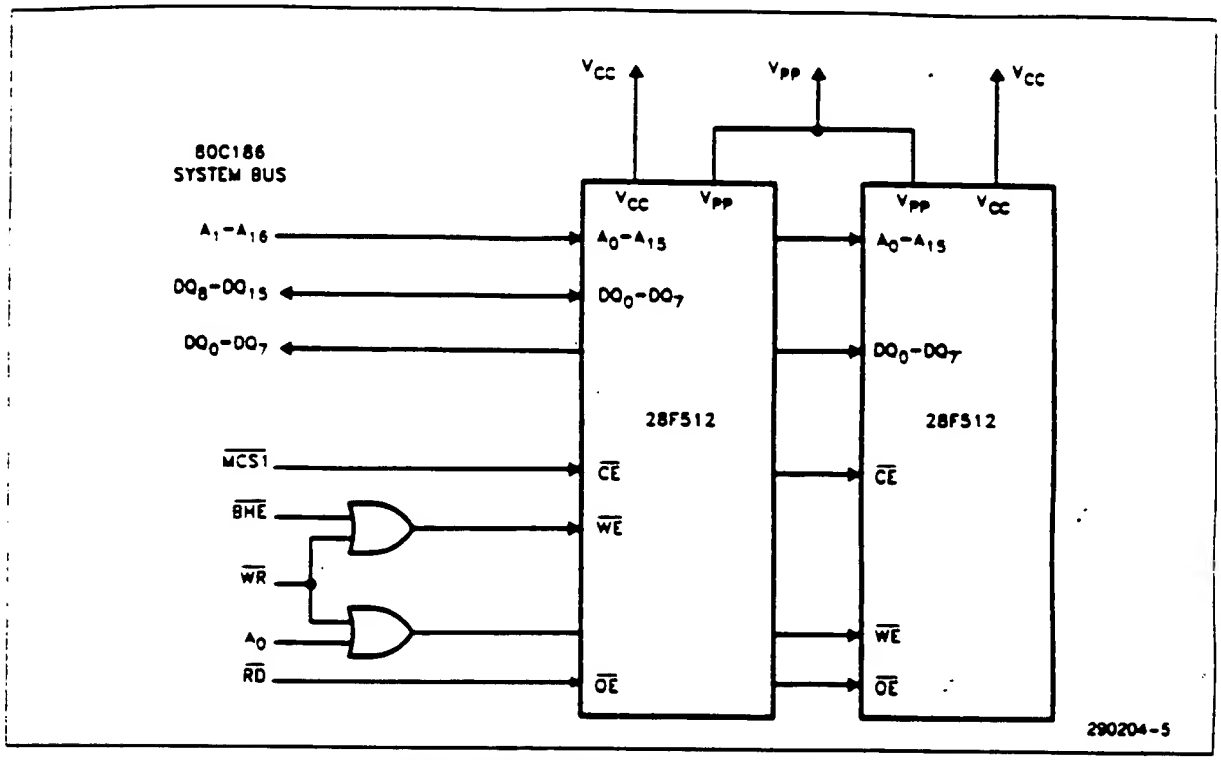


Figure 3. 28F512 in a 80C186 System

With cost-effective in-system reprogramming and extended cycling capability, the 28F512 fills the functionality gap between traditional EPROMs and E²PROMs. EPROM-compatible specifications, straightforward interfacing, and in-circuit alterability allows designers to easily augment memory flexibility and satisfy the need for updatable nonvolatile storage in today's designs.

PRINCIPLES OF OPERATION

Flash-memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 28F512 introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 28F512 is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and int$_e$ligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—int$_e$ligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the int$_e$ligent Identifier codes, or output data for erase and program verification.

The command register is only alterable when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When high voltage is removed,

SAN040006

Table 2. 28F512 Bus Operations

Operation	Pins	V_{PP}(1)	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	int$_e$ligent Identifier™ (Mfr)(2)	V_{PPL}	V_{IL}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	int$_e$ligent Identifier™ (Device)(2)	V_{PPL}	V_{IH}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = B8H
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out(4)
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby(5)	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In(6)

NOTES:
1. V_{PPL} may be ground, a no-connect with a resistor tied to ground, or $\leq V_{CC} - 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to D.C. Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. V_{ID} is the int$_e$ligent Identifier high voltage. Refer to DC Characteristics.
4. Read operations with $V_{PP} = V_{PPH}$ may access array data or the int$_e$ligent Identifier™ codes.
5. With V_{PP} at high voltage, the standby current equals $I_{CC} - I_{PP}$ (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V_{IL} or V_{IH}.

the contents of the register default to the read command, making the 28F512 a read-only memory. Memory contents cannot be altered.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this instance, all operations are performed in conjunction with the command register. The 28F512 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read

The 28F512 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Figure 6 illustrates read timing waveforms.

When V_{PP} is high (V_{PPH}), the read operation can be used to access array data, to output the int$_e$ligent ...tifier™ codes, and to access data for program/...e verification. When V_{PP} is low (V_{PPL}), the read operation can only access the array data.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 28F512's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. If the 28F512 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

int$_e$ligent Identifier™ Operation

The int$_e$ligent Identifier operation outputs the manufacturer code (89H) and device code (B8H). Programming equipment automatically matches the device with its proper erase and programming algorithms.

SAN040007

With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage V_{ID} (see DC Characteristics) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 28F512 is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B8H).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

Refer to A.C. Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 28F512 register commands.

Table 3. Command Definitions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read Intelligent Identifier™ Code(4)	2	Write	X	90H	Read	IA	ID
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification (Mfr = 89H, Device = B8H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
5. Figure 5 illustrates the Quick-Erase™ algorithm.
6. Figure 4 illustrates the Quick-Pulse Programming™ algorithm.
7. The second bus cycle must be followed by the desired command register write.

SAN040008

Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the 28F512, the device powers-up and remains enabled for reads until the command-register contents are changed. Refer to the A.C. Read Characteristics and Waveforms for specific timing parameters.

inteligent Identifier™ Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The 28F512 contains an inteligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of B8H. To terminate the operation, it is necessary to write another valid command into the register.

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to A.C. Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 28F512 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. Figure 5, the Quick-Erase™ algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F512. Refer to A.C. Erase Characteristics and Waveforms for specific timing parameters.

Set-up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to A.C. Program-

ming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command

The 28F512 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The 28F512 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 4, the 28F512 Quick-Pulse Programming™ algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to A.C. Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX-II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wearout by a factor of 100,000,000.

The 28F512 is specified for a minimum of 10,000 program/erase cycles. The device is programmed and erased using Intel's Quick-Pulse Programming™ and Quick-Erase™ algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 10 µs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 4 illustrates the Quick-Pulse Programming algorithm.

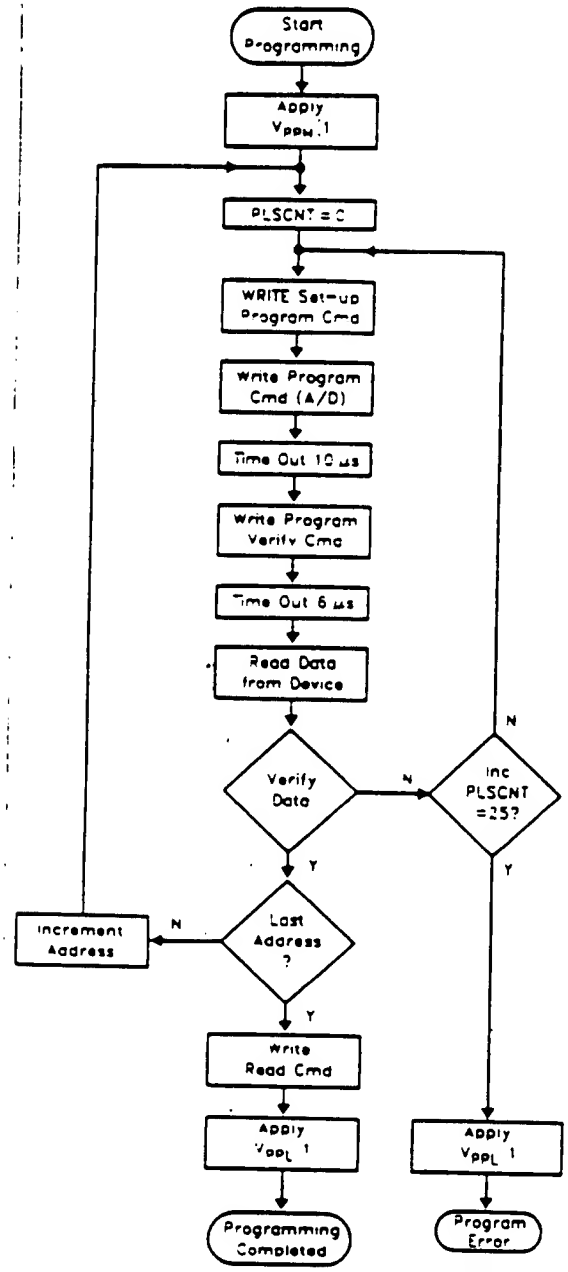
QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The 28F512 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately one second.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 5 illustrates the Quick-Erase algorithm.



290204-6

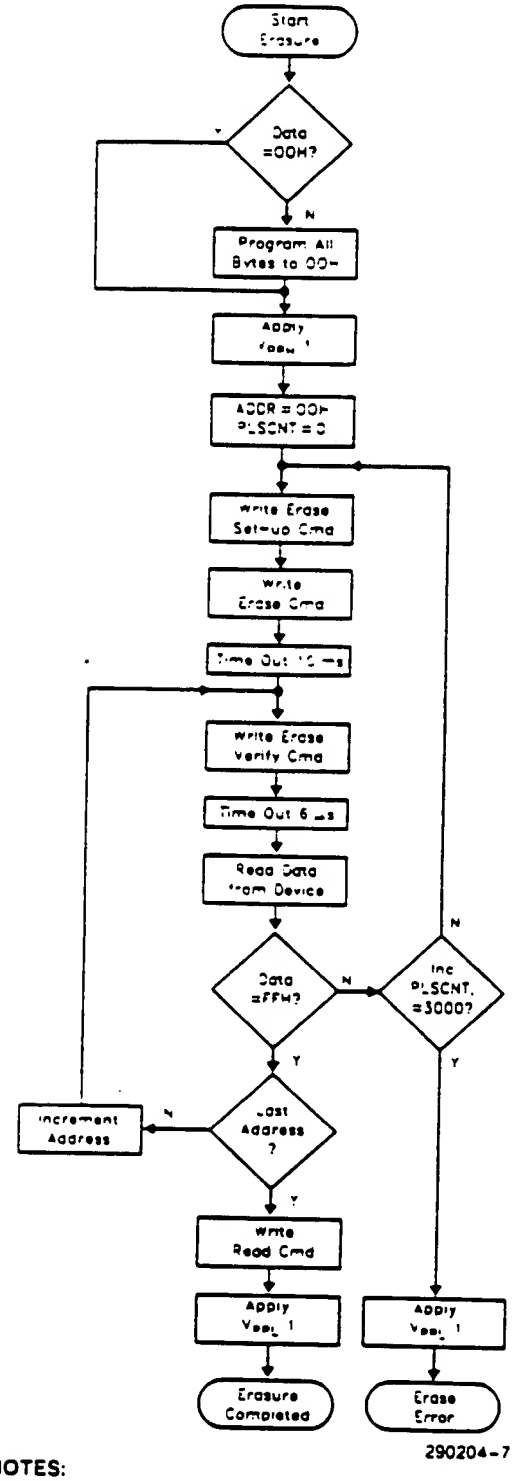
Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H; Stops Program Operation
Standby		t_{WHGL}
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H. Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:

1. See D.C. Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or less than V_{CC} + 2.0V. Refer to Principles of Operation.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 4. 28F512 Quick-Pulse Programming™ Algorithm

SAN040011



290204-7

Bus Operation	Command	Comments
		Entire memory must = 00H before erasure
		Use Quick-Pulse Programming™ Algorithm (Figure 4)
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Addresses and Pulse-Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase Verify	Addr = Byte to Verify; Data = A0H; Stops Erase Operation
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse-Count
Write	Read	Data = 00H. Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

SAN040012

NOTES:

1. See D.C. Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or less than V_{CC} + 2.0V. Refer to Principles of Operation.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.
3. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 5. 28F512 Quick-Erase™ Algorithm

DESIGN CONSIDERATIONS

Two-Line Output Control

Flash-memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation and,
b. complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash-memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Sequencing

The 28F512 is designed to offer protection against accidental erasure or programming, caused by spurious system-level signals that may exist during power transitions. The 28F512 powers-up in its read-only state. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of the two-step command sequences. While these precautions are sufficient for most applications, it is recommended that V_{CC} reach its steady-state value before raising V_{PP} above V_{CC} − 2.0V. In addition, upon powering-down, V_{PP} should be below V_{CC} − 2.0V, before lowering V_{CC}.

SAN040013

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
- During Read ..... 0°C to +70°C(1)
- During Erase/Program ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
Voltage on Any Pin with Respect to Ground ..... −2.0V to +7.0V(2)
Voltage on Pin A_9 with Respect to Ground ..... −2.0V to +13.5V(2, 3)
V_{PP} Supply Voltage with Respect to Ground During Erase/Program .... −2.0V to +14.0V(2, 3)
V_{CC} Supply Voltage with Respect to Ground ..... −2.0V to +7.0V(2)
Output Short Circuit Current ..... 100 mA(4)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum D.C. input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum D.C. voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current		±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current		1.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$
I_{CC1}(1)	V_{CC} Active Read Current		30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}(1)	V_{CC} Programming Current		30	mA	Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current		30	mA	Erasure in Progress
I_{PPS}	V_{PP} Leakage Current		±10	µA	$V_{PP} = V_{PPL}$

SAN040014

D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE (Continued)

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
			±10		$V_{PP} = V_{PPL}$
I_{PP2}[2]	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}[2]	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} − 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage	2.4		V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min
V_{ID}	A9 Intelligent Identifer™ Voltage	11.50	13.00	V	
I_{ID}	A9 Intelligent Identifier™ Current		500	µA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations	0.00	V_{CC} − 2.0V	V	**NOTE:** Erase/Program are inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations	11.40	12.60	V	

D.C. CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Limits Min	Limits Max	Unit	Test Conditions
I_{LI}	Input Leakage Current		±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current		±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current		100	µA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} \pm 0.2V$
I_{CC1}[1]	V_{CC} Active Read Current		30	mA	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IL}$ f = 6 MHz. I_{OUT} = 0 mA
I_{CC2}[1]	V_{CC} Programming Current		30	mA	Programming in Progress
I_{CC3}[1]	V_{CC} Erase Current		30	mA	Erasure in Progress
I_{PPS}	V_{PP} Leakage Current		±10	µA	$V_{PP} = V_{PPL}$

SAN040015

D.C. CHARACTERISTICS—CMOS COMPATIBLE (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
			±10		$V_{PP} = V_{PPL}$
I_{PP2}(2)	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}(2)	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} − 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage	0.85 V_{CC}		V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ Min
V_{OH2}		V_{CC} − 0.4			I_{OH} = −100 µA, $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifer™ Voltage	11.50	13.00	V	
I_{ID}	A_9 intelligent Identifier™ Current		500	µA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations	0.00	V_{CC} + 2.0V	V	**NOTE:** Erase/Programs are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations	11.40	12.60	V	

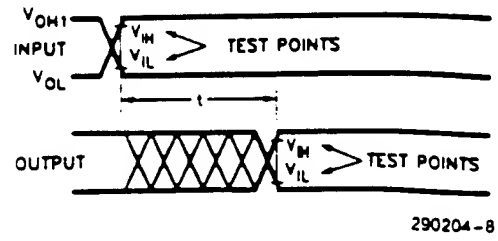
CAPACITANCE(3) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Limits		Unit	Conditions
		Min	Max		
C_{IN}	Address/Control Capacitance		6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

NOTES:
1. Active I_{CC} current of a typical device is 12 mA with nominal V_{CC} at room temperature.
2. Active I_{PP} current of a typical device is 10 mA with nominal V_{PP} at room temperature.
3. Sampled, not 100% tested.

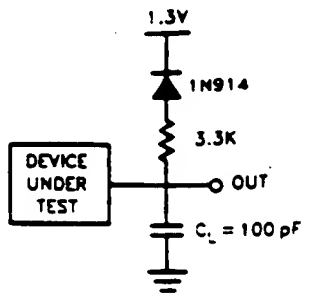
SAN040016

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at V_{OH1} for a logic "1" and V_{OL} for a logic "0". Testing measurements are made at V_{IH} for a logic "1" and V_{IL} for a logic "0". Rise/Fall time ≤ 10 ns.

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

A.C. TEST CONDITIONS

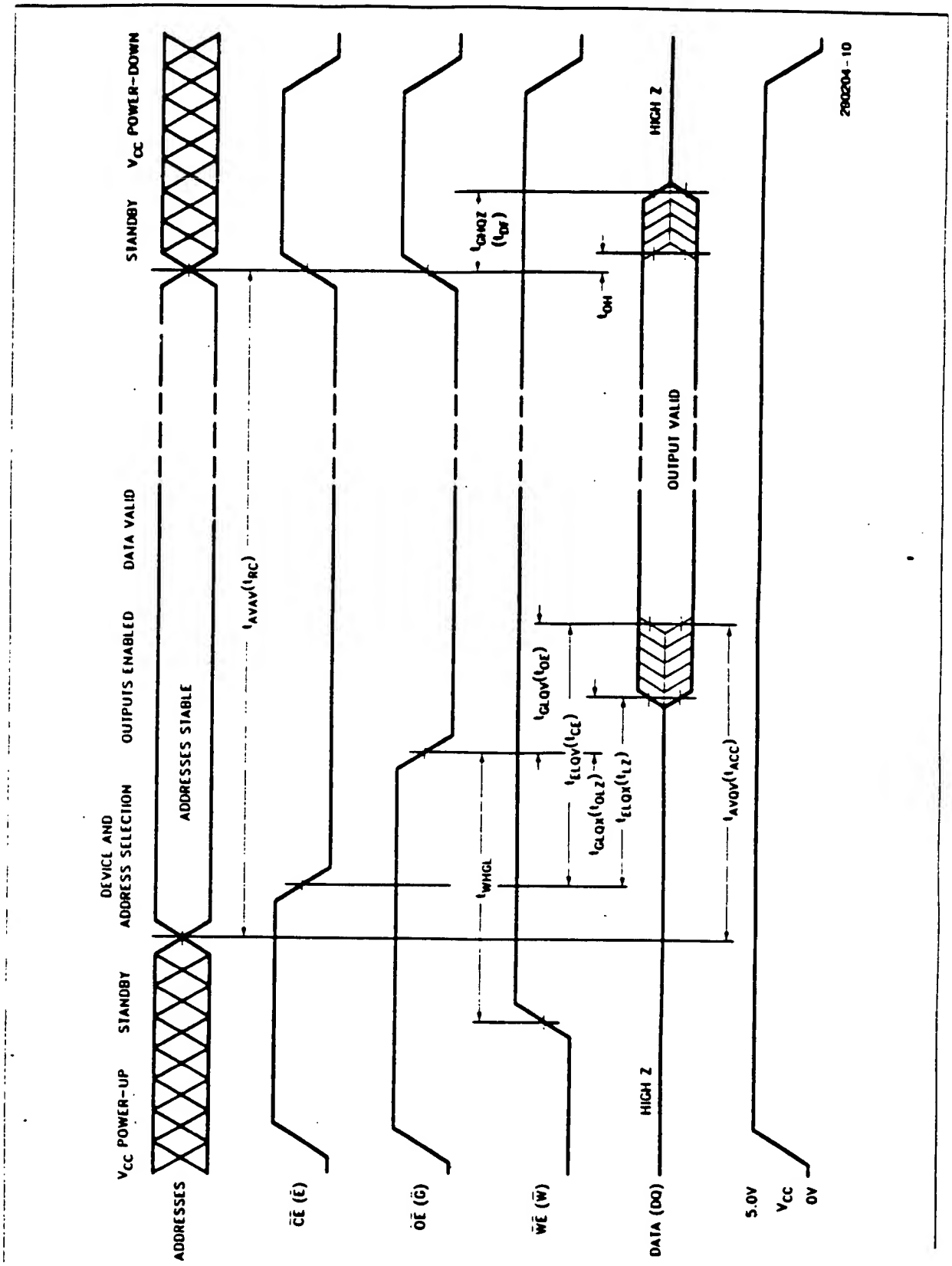
Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... V_{OL} and V_{OH1}
Input Timing Reference Level ..... V_{IL} and V_{IH}
Output Timing Reference Level ..... V_{IL} and V_{IH}

A.C. CHARACTERISTICS—Read-Only Operations

Versions		28F512-120 P1C4		28F512-150 P1C4		28F512-200 P1C4		Unit
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time	120		150		200		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time		120		150		200	ns
t_{AVQV}/t_{ACC}	Address Access Time		120		150		200	ns
t_{GLQV}/t_{OE}	Output Enable Access Time		50		55		60	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	0		0		0		ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	0		0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z		30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change[1]	0		0		0		ns
t_{WHGL}	Write Recovery Time before Read	6		6		6		µs

NOTES:
1. Whichever occurs first.
2. Rise/Fall Time ≤ 10 ns.

SAN040017



SAN040018

Figure 6. A.C. Waveforms for Read Operations

A.C. CHARACTERISTICS—Write/Erase/Program Operations(1)

Versions		28F512-120 P1C4		28F512-150 P1C4		28F512-200 P1C4		Unit
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time	120		150		200		ns
t_{AVWL}/t_{AS}	Address Set-Up Time	0		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time	60		60		75		ns
t_{DVWH}/t_{DS}	Data Set-up Time	50		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time	10		10		10		ns
t_{WHGL}	Write Recovery Time before Read	6		6		6		µs
t_{GHWL}	Read Recovery Time before Write	0		0		0		µs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time before Write	20		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time	0		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width(2)	50		50		60		ns
t_{ELEH}	Alternative Write(2) Pulse Width	70		70		80		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High	20		20		20		ns
t_{WHWH1}	Duration of Programming Operation	10	25	10	25	10	25	µs
t_{WHWH2}	Duration of Erase Operation	9.5	10.5	9.5	10.5	9.5	10.5	ms
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low	100		100		100		ns

NOTES:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to A.C. Characteristics for Read-Only Operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (within a longer Write-Enable timing waveform) all set-up, hold, and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. Rise/Fall time ≤ 10 ns.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Chip Erase Time		0.5(1)	30	Sec	Excludes 00H Programming Prior to Erasure
Chip Program Time		1(1)	12(2)	Sec	Excludes System-Level Overhead
Erase/Program Cycles(3)	10,000	100,000		Cycles	

NOTES:
1. 25°C, 12.0V V_{PP}, 10,000 cycles.
2. Minimum byte programming time excluding system overhead is 16 µs (10 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs * 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Refer to AR-60 "ETOX™ Flash Memory Reliability Data Summary" for typical cycling data and failure rate calculations.

SAN040019

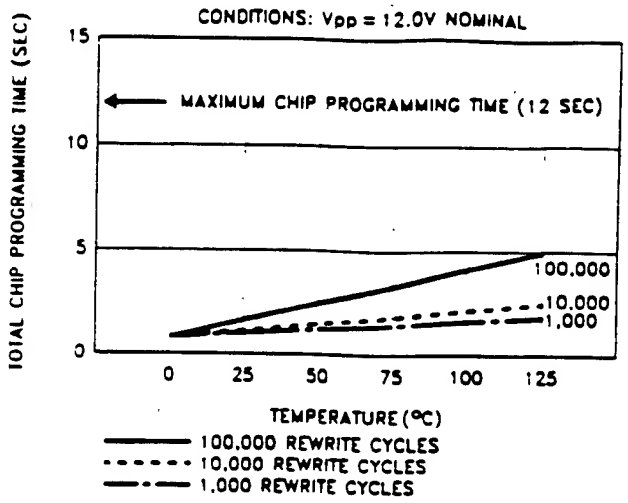


Figure 7. 28F512 Typical Programming Time vs. Temperature

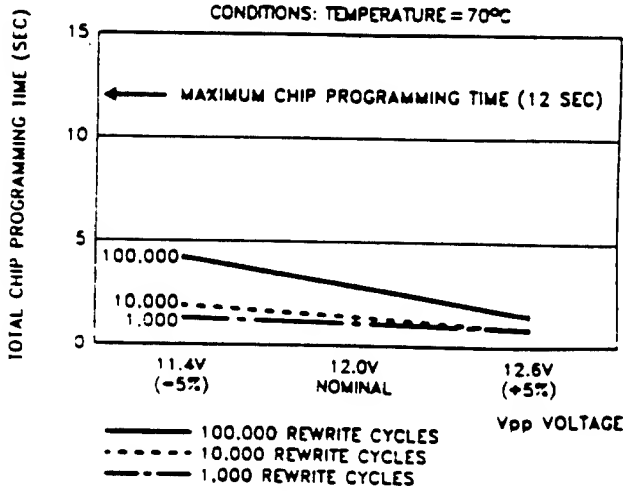


Figure 8. 28F512 Typical Programming Time vs. Vpp Voltage

SAN040020

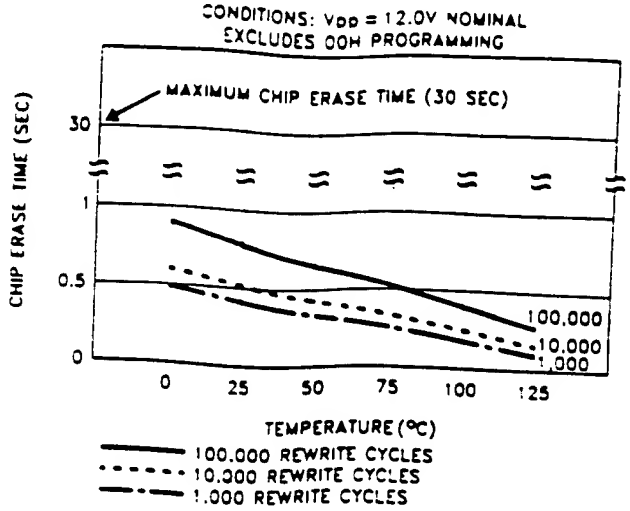


Figure 9. 28F512 Typical Erase Time vs. Temperature

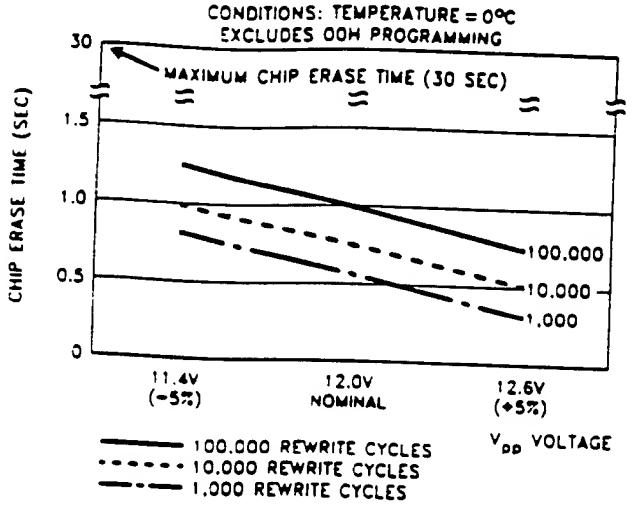


Figure 10. 28F512 Typical Erase Time vs. V_{PP} Voltage

SAN040021

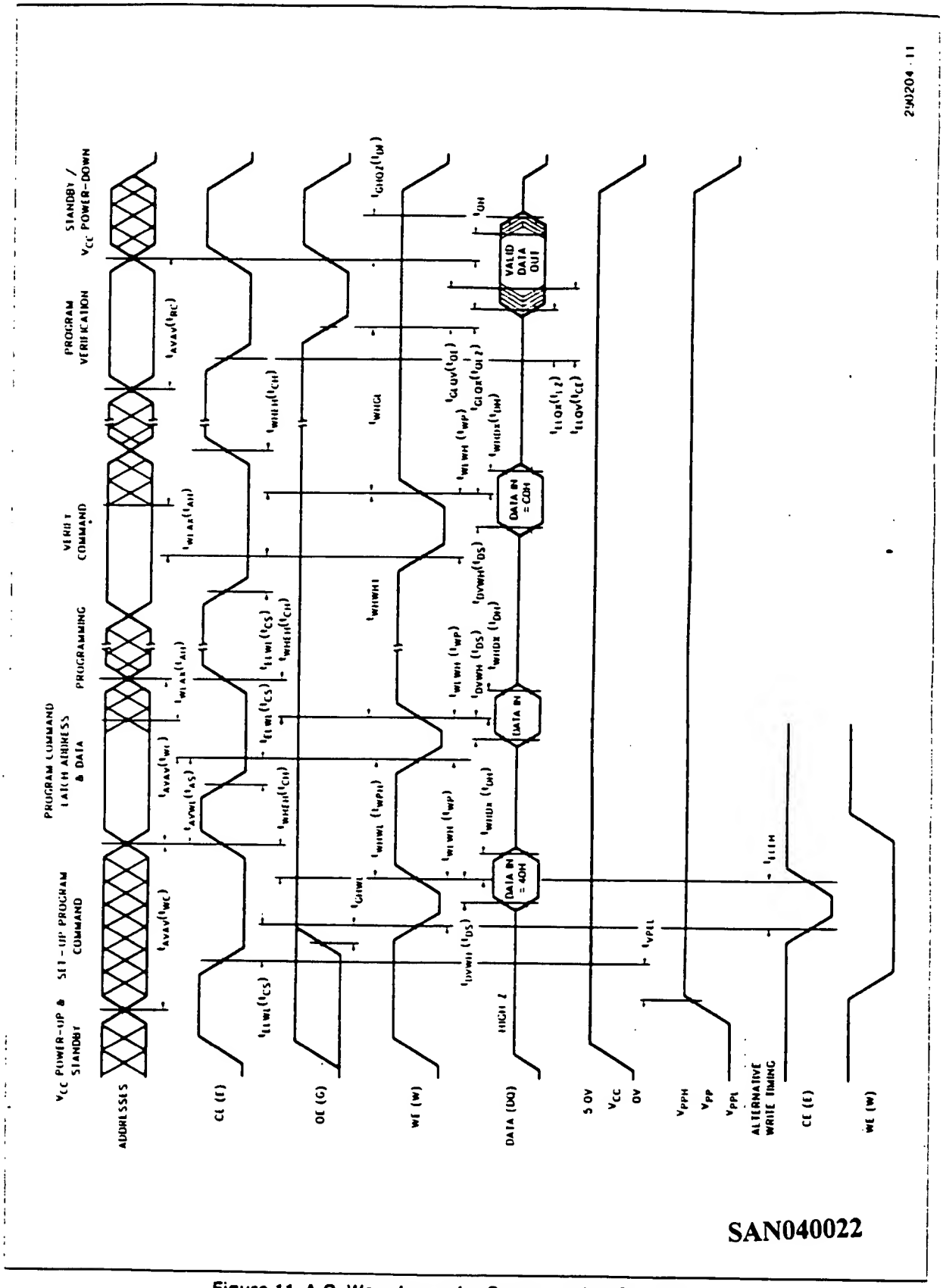


Figure 11. A.C. Waveforms for Programming Operations

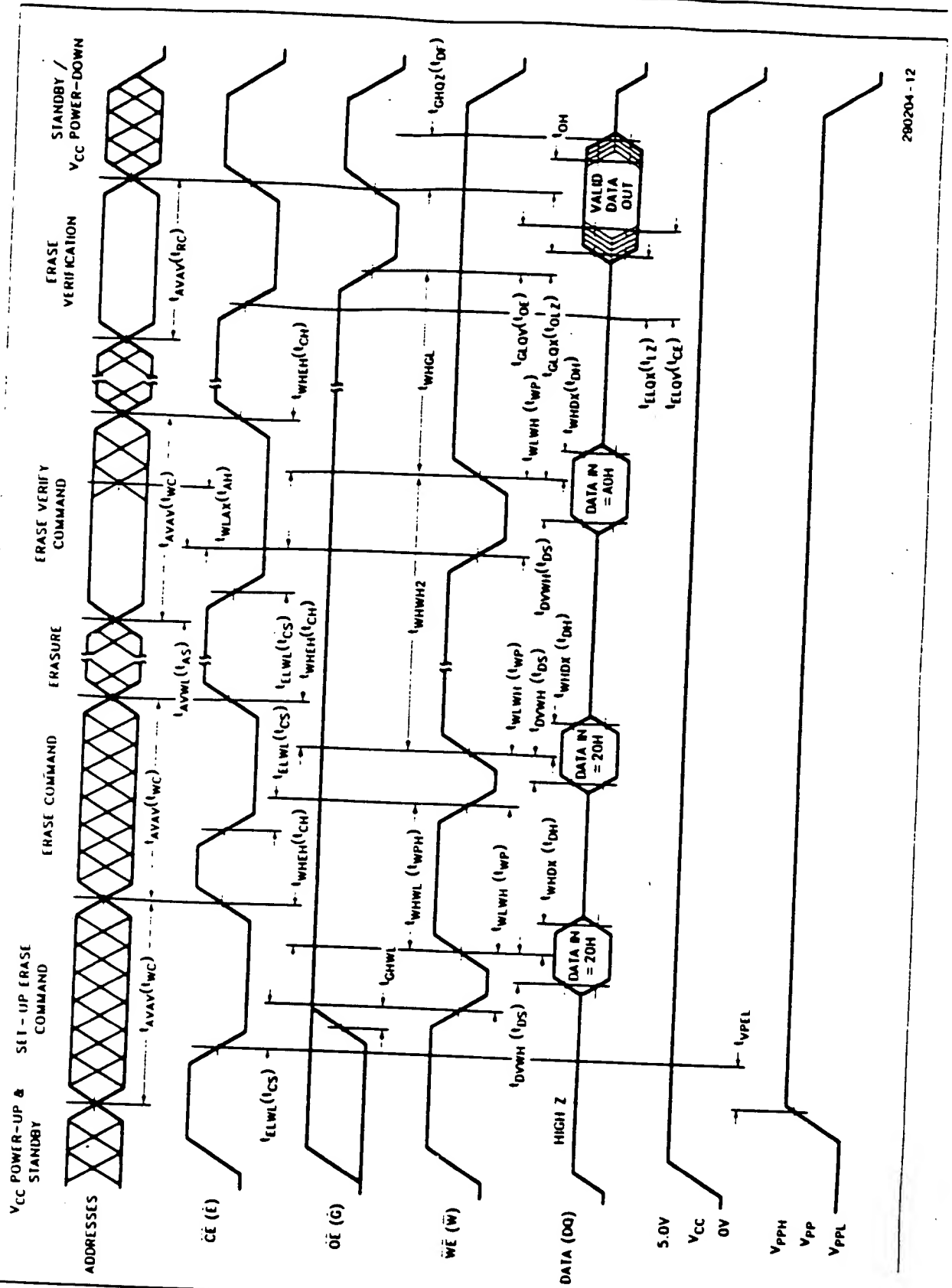


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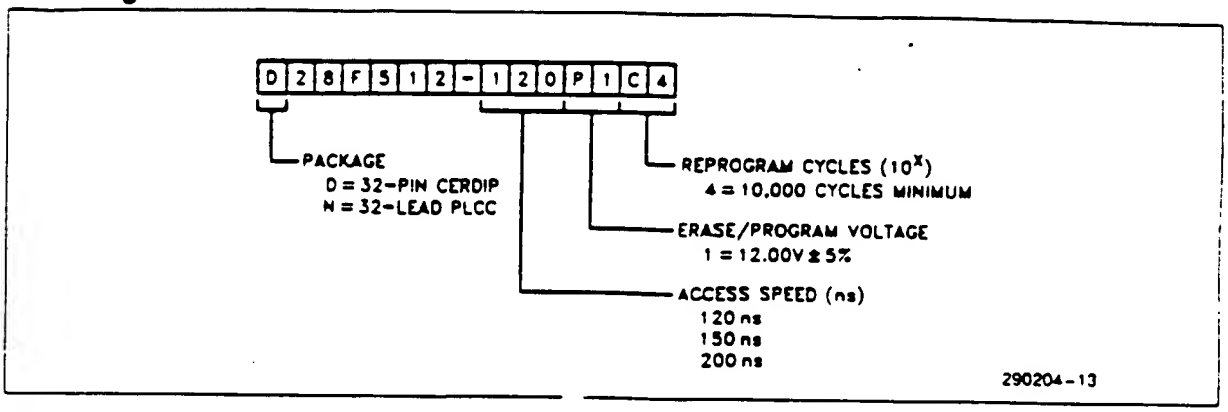
Figure 12. A.C. Waveforms for Erase Operations

Ordering Information



Valid Combinations:

D28F512-120P1C4	N28F512-120P1C4
D28F512-150P1C4	N28F512-150P1C4
D28F512-200P1C4	N28F512-200P1C4

ADDITIONAL INFORMATION

	Order Number
ER-20, "ETOX™ Flash Memory Technology"	294005
ER-23, "The Intel 28F512 Flash Memory"	294007
RR-60, "ETOX™ Flash Memory Reliability Data Summary"	293002
AP-316, "Using Flash Memory for In-System Reprogrammable Nonvolatile Storage"	292046

SAN040024

intel

PRELIMINARY

28F010
1024K (128K x 8) CMOS FLASH MEMORY

- Flash Electrical Chip-Erase
  - 1 Second Typical Chip-Erase
- Quick-Pulse Programming™ Algorithm
  - 10 μs Typical Byte-Program
  - 2 Second Chip-Program
- 10,000 Erase/Program Cycles Minimum
- 12.0V ±5% V_{PP}
- High-Performance Read
  - 135 ns Maximum Access Time
- CMOS Low Power Consumption
  - 30 mA Maximum Active Current
  - 100 μA Maximum Standby Current
- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- Noise Immunity Features
  - ±10% V_{CC} Tolerance
  - Maximum Latch-Up Immunity through EPI Processing
- ETOX™-II Flash-Memory Technology
  - EPROM-Compatible Process Base
  - High-Volume Manufacturing Experience
- Compatible with JEDEC-Standard Byte-Wide EPROM Pinouts
  - 32-Pin Cerdip
  - 32-Lead PLCC

(See Packaging Spec., Order # 231369)

Intel's 28F010 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F010 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F010 increases memory flexibility, while contributing to time- and cost-savings.

The 28F010 is a 1024-kilobit nonvolatile memory organized as 131,072 bytes of 8 bits. Intel's 28F010 is offered in 32-pin cerdip or 32-lead PLCC packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Extended erase and program cycling capability is designed into Intel's ETOX-II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F010 performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming™ and Quick-Erase™ algorithms.

Intel's 28F010 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 135 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 μA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from −1V to V_{CC} + 1V.

With Intel's ETOX-II process base, the 28F010 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

SAN040025

October 1989
Order Number: 290207-003

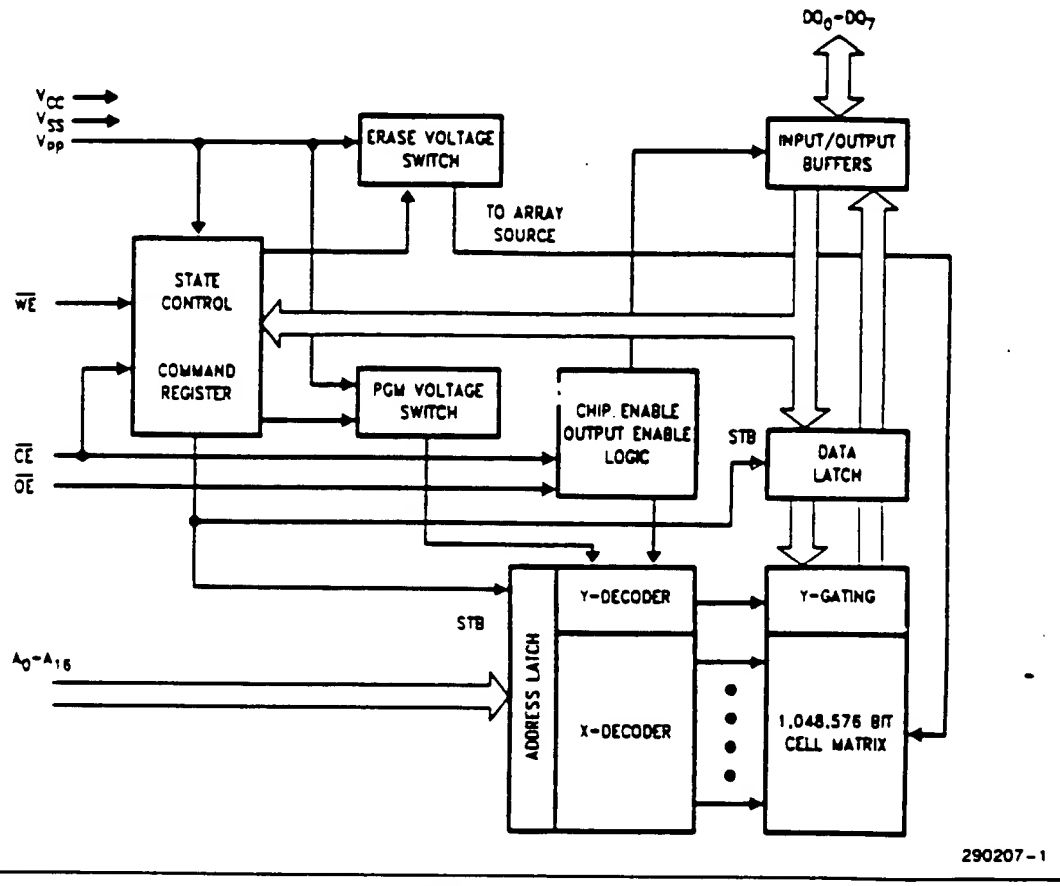


Figure 1. 28F010 Block Diagram

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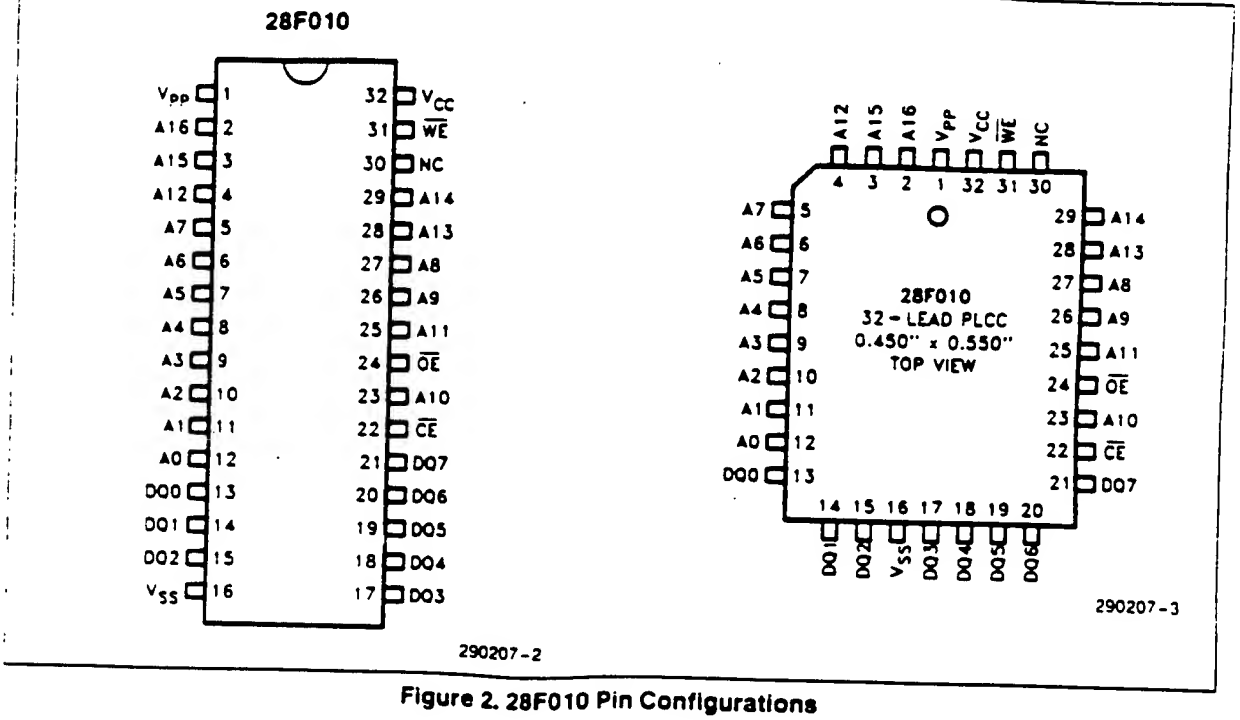

Figure 2. 28F010 Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{16}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers, decoders and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{OE}$	INPUT	**OUTPUT ENABLE:** Gates the devices output through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	**WRITE ENABLE:** Controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the $\overline{WE}$ pulse. **Note:** With $V_{PP} \leq V_{CC} - 2V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY** (5V ± 10%)
V_{SS}		**GROUND**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.

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APPLICATIONS

The 28F010 flash-memory adds electrical chip-erasure and reprogrammability to EPROM non-volatility and ease of use. The 28F010 is ideal for storing code or data-tables in applications where periodic updates are required. With a minimum of 10,000 erase/program cycles, the 28F010 also serves as a dense, nonvolatile data acquisition and storage medium.

The need for code updates pervades all phases of a system's life—from prototyping to system manufacture to after-sale service. In the factory, during prototyping, revisions to control code necessitate ultraviolet erasure and reprogramming of EPROM-based prototype codes. The 28F010 replaces the 15- to 20-minute ultraviolet erasure with one-second electrical erasure. Electrical chip-erasure and reprogramming occur in the same workstation or PROM-programmer socket.

Diagnostics, performed at subassembly or final assembly stages, often require the socketing of EPROMs. Socketed test codes are ultimately replaced with EPROMs containing the final program. With electrical chip-erasure and reprogramming, the 28F010 is soldered to the circuit board. Test codes are programmed into the 28F010 as it resides on the circuit board. Ultimately, the final code can be downloaded to the device. The 28F010's in-circuit alterability eliminates unnecessary handling and less-reliable socketed connections, while adding greater test flexibility.

Material and labor costs associated with code changes increase at higher levels of system integration—the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revisions to EPROM-based code require the removal of EPROM components or entire boards. The service technician performs the twenty-minute ultraviolet erasure and reprogramming on-site, or returns boards to the factory for rework. An alternate approach is to use one-time-programmable EPROMs. The service technician removes the "old" devices and replaces them with updated versions. The used components are discarded.

Designing with the in-circuit alterable 28F010 eliminates socketed memories, reduces overall material costs, and drastically cuts the labor costs associated with code updates. With the 28F010, code updates are implemented locally via an edge-connector, or remotely over a serial communication link.

The 28F010's electrical chip-erasure, byte reprogrammability, and complete nonvolatility fit well with data accumulation needs. Electrical chip-erasure gives the designer a "blank-slate" in which to log data. Data can be periodically off-loaded for analysis—erasing the slate and repeating the cycle. Or, multiple devices can maintain a "rolling window" of accumulated data.

With high density, nonvolatility, and extended cycling capability, the 28F010 offers an innovative alternative for mass storage. Integrating main memory and backup storage functions into directly executable flash memory boosts system performance, shrinks system size, and cuts power consumption. Reliability exceeds that of electromechanical media, with greater durability in extreme environmental conditions.

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 depicts two 28F010s tied to the 80C186 system bus. The 28F010's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

With cost-effective in-system reprogramming and extended cycling capability, the 28F010 fills the functionality gap between traditional EPROMs and E^{2}PROMs. EPROM-compatible specifications, straightforward interfacing, and in-circuit alterability allows designers to easily augment memory flexibility and satisfy the need for updatable nonvolatile storage in today's designs.

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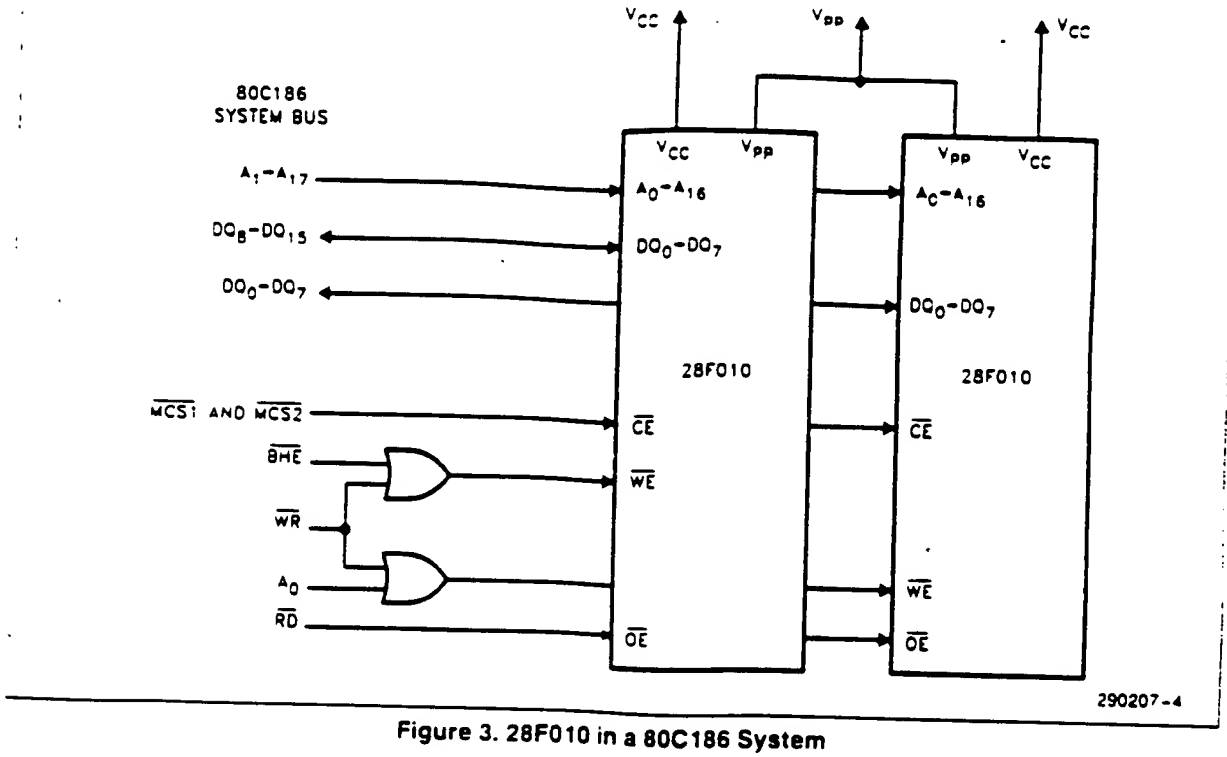

Figure 3. 28F010 in a 80C186 System

PRINCIPLES OF OPERATION

Flash-memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 28F010 introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supplies during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 28F010 is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and Int$_e$ligent Identifier™ operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—Int$_e$ligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming or erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the Int$_e$ligent Identifier codes, or output data for erase and program verification.

The command register is only alterable when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When high voltage is removed,

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Table 2. 28F010 Bus Operations

Operation	Pins	V_{PP}[1]	A_0	A_9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	int$_e$ligent Identifier™ (Mfr)[2]	V_{PPL}	V_{IL}	V_{ID}[3]	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	int$_e$ligent Identifier™ (Device)[2]	V_{PPL}	V_{IH}	V_{ID}[3]	V_{IL}	V_{IL}	V_{IH}	Data = B4H
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out[4]
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby[5]	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In[6]

NOTES:
1. V_{PPL} may be ground, a no-connect with a resistor tied to ground, or ≤ V_{CC} + 2.0V. V_{PPH} is the programming voltage specified for the device. Refer to D.C. Characteristics. When V_{PP} = V_{PPL} memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. V_{ID} is the int$_e$ligent Identifier high voltage. Refer to DC Characteristics.
4. Read operations with V_{PP} = V_{PPH} may access array data or the int$_e$ligent Identifier™ codes.
5. With V_{PP} at high voltage, the standby current equals I_{CC} + I_{PP} (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V_{IL} or V_{IH}.

the contents of the register default to the read command, making the 28F010 a read-only memory. Memory contents cannot be altered.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this instance, all operations are performed in conjunction with the command register. The 28F010 is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

BUS OPERATIONS

Read

The 28F010 has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable ($\overline{CE}$) is the power control and should be used for device selection. Output-Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Figure 6 illustrates read timing waveforms.

When V_{PP} is high (V_{PPH}), the read operation can be used to access array data, to output the int$_e$ligent Identifier™ codes, and to access data for program/erase verification. When V_{PP} is low (V_{PPL}), the read operation can **only** access the array data.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 28F010's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance state, independent of the Output-Enable signal. If the 28F010 is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

int$_e$ligent Identifier™ Operation

The int$_e$ligent Identifier operation outputs the manufacturer code (89H) and device code (B4H). Programming equipment automatically matches the device with its proper erase and programming algorithms.

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With Chip-Enable and Output-Enable at a logic low level, raising A9 to high voltage V_{ID} (see DC Characteristics) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 28F010 is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B4H).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

Refer to A.C. Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 28F010 register commands.

Table 3. Command Definitions

Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
	Req'd	Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read Intelligent Identifier™ Codes(4)	2	Write	X	90H	Read	IA	ID
Set-up Erase/Erase(5)	2	Write	X	20H	Write	X	20H
Erase Verify(5)	2	Write	EA	A0H	Read	X	EVD
Set-up Program/Program(6)	2	Write	X	40H	Write	PA	PD
Program Verify(6)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification (Mfr = 89H, Device = B4H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
5. Figure 5 illustrates the Quick-Erase™ Algorithm.
6. Figure 4 illustrates the Quick-Pulse Programming™ Algorithm.
7. The second bus cycle must be followed by the desired command register write.

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Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alteration of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the 28F010, the device powers-up and remains enabled for reads until the command-register contents are changed. Refer to the A.C. Read Characteristics and Waveforms for specific timing parameters.

int$_e$ligent Identifier™ Command

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The 28F010 contains an int$_e$ligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code of 89H. A read cycle from address 0001H returns the device code of B4H. To terminate the operation, it is necessary to write another valid command into the register.

Set-up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erasure of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register.

To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence of this high voltage, memory contents are protected against erasure. Refer to A.C. Erase Charactenstics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 28F010 applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. Figure 5, the Quick-Erase™ algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F010. Refer to A.C. Erase Characteristics and Waveforms for specific timing parameters.

Set-up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to A.C. Program-

ming Characteristics and Waveforms for specific timing parameters.

Program-Verify Command

The 28F010 is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The 28F010 applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 4, the 28F010 Quick-Pulse Programming™ algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to A.C. Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX-II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower than EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wearout by a factor of 100,000,000.

The 28F010 is specified for a minimum of 10,000 program/erase cycles. The device is programmed and erased using Intel's Quick-Pulse Programming™ and Quick-Erase™ algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm uses programming operations of 10 µs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 4 illustrates the Quick-Pulse Programming algorithm.

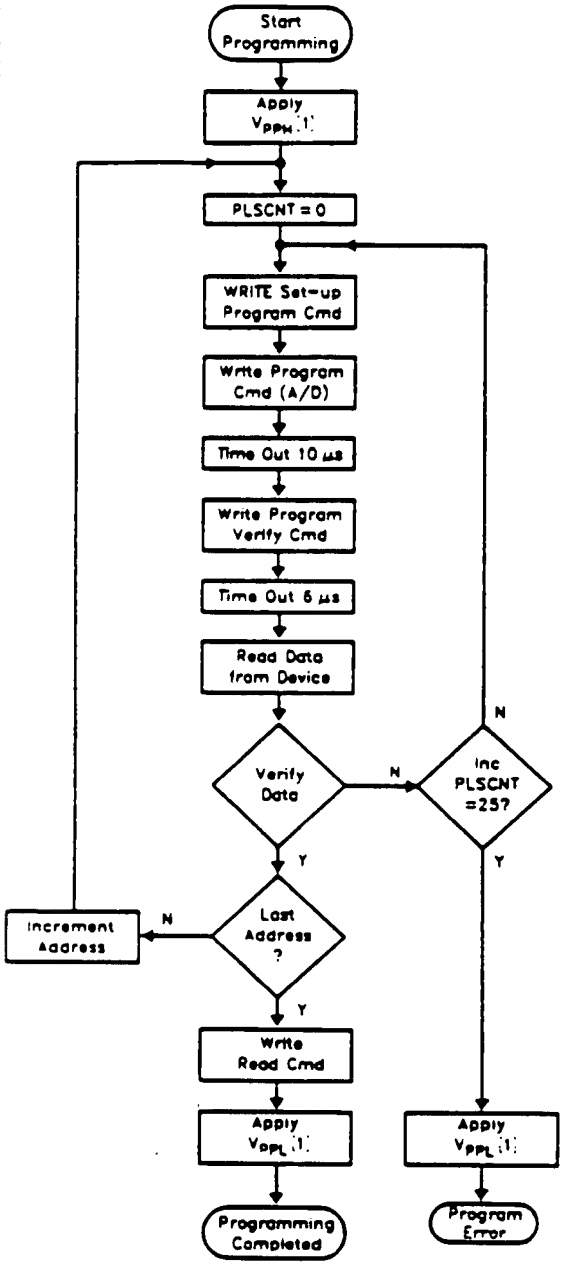
QUICK-ERASE™ ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming™ algorithm, to simultaneously remove charge from all bits in the array.

Erasure begins with a read of memory contents. The 28F010 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately two seconds.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 5 illustrates the Quick-Erase algorithm.



290207-5

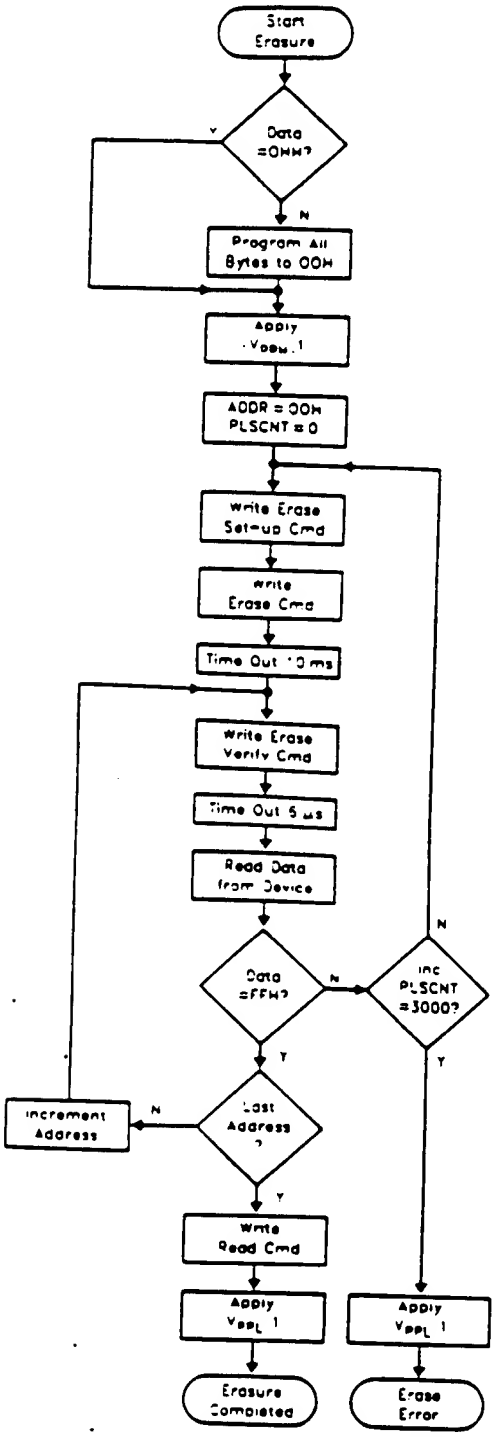
Bus Operation	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Pulse-Count
Write	Set-up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Program Operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H; Stops Program Operation
Standby		t_{WHGL}
Read		Read Byte to Verify Programming
Standby		Compare Data Output to Data Expected
Write	Read	Data = 00H, Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:

1. See D.C. Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or less than V_{CC} − 2.0V. Refer to Principles of Operation.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 4. 28F010 Quick-Pulse Programming™ Algorithm

SAN040034



290207-6

Bus Operation	Command	Comments
		Entire Memory Must = 00H Before Erasure
		Use Quick-Pulse Programming™ Algorithm (Figure 4)
Standby		Wait for V_{PP} Ramp to V_{PPH}(1)
		Initialize Addresses and Pulse-Count
Write	Set-up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase Verify	Addr = Byte to Verify; Data = A0H: Stops Erase Operation
Standby		t_{WHGL}
Read		Read Byte to Verify Erasure
Standby		Compare Output to FFH Increment Pulse-Count
Write	Read	Data = 00H. Resets the Register for Read Operations
Standby		Wait for V_{PP} Ramp to V_{PPL}(1)

NOTES:

1. See D.C. Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no-connect with a resistor tied to ground, or less than V_{CC} – 2.0V. Refer to Principles of Operation.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the read command.
3. **CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.**

Figure 5. 28F010 Quick-Erase™ Algorithm

DESIGN CONSIDERATIONS

Two-Line Output Control

Flash-memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation and,
b. complete assurance that output bus contention will not occur.

To efficiently use these two control inputs, an address-decoder output should drive chip-enable, while the system's read signal controls all flash-memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash-memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash-memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Sequencing

The 28F010 is designed to offer protection against accidental erasure or programming, caused by spurious system-level signals that may exist during power transitions. The 28F010 powers-up in its read-only state. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of the two-step command sequences. While these precautions are sufficient for most applications, it is recommended that V_{CC} reach its steady-state value before raising V_{PP} above V_{CC} – 2.0V. In addition, upon powering-down, V_{PP} should be below V_{CC} – 2.0V, before lowering V_{CC}.

SAN040036

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
- During Read ..... 0°C to +70°C(1)
- During Erase/Program ..... 0°C to +70°C

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +125°C
Voltage on Any Pin with
- Respect to Ground ..... −2.0V to +7.0V(2)

Voltage on Pin A_9 with
- Respect to Ground ..... −2.0V to −13.5V(2, 3)

V_{PP} Supply Voltage with
- Respect to Ground
- During Erase/Program .... −2.0V to +14.0V(2, 3)

V_{CC} Supply Voltage with
- Respect to Ground ..... −2.0V to +7.0V(2)

Output Short Circuit Current ..... 100 mA(4)

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended penods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum D.C. input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} − 0.5V, which may overshoot to V_{CC} − 2.0V for periods less than 20 ns.
3. Maximum D.C. voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current		±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current		1.0	mA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$
I_{CC1}(1)	V_{CC} Active Read Current		30	mA	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}(1)	V_{CC} Programming Current		30	mA	Programming in Progress
I_{CC3}(1)	V_{CC} Erase Current		30	mA	Erasure in Progress
I_{PPS}	V_{PP} Leakage Current		±10	µA	$V_{PP} = V_{PPL}$

SAN040037

D.C. CHARACTERISTICS—TTL/NMOS COMPATIBLE (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
			±10		$V_{PP} = V_{PPL}$
I_{PP2}[2]	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}[2]	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage	2.4		V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifer™ Voltage	11.50	13.00	V	
I_{ID}	A_9 intelligent Identifier™ Current		500	µA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations	0.00	V_{CC} + 2.0V	V	**NOTE:** Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations	11.40	12.60	V	

D.C. CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{LI}	Input Leakage Current		±1.0	µA	$V_{CC} = V_{CC}$ Max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current		±10	µA	$V_{CC} = V_{CC}$ Max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current		100	µA	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} \pm 0.2V$
I_{CC1}[1]	V_{CC} Active Read Current		30	mA	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IL}$ f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}[1]	V_{CC} Programming Current		30	mA	Programming in Progress
I_{CC3}[1]	V_{CC} Erase Current		30	mA	Erasure in Progress
I_{PPS}	V_{PP} Leakage Current		±10	µA	$V_{PP} = V_{PPL}$

SAN040038

D.C. CHARACTERISTICS—CMOS COMPATIBLE (Continued)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min	Max		
I_{PP1}	V_{PP} Read Current		200	µA	$V_{PP} = V_{PPH}$
			±10		$V_{PP} = V_{PPL}$
I_{PP2}(2)	V_{PP} Programming Current		30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}(2)	V_{PP} Erase Current		30	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} − 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min
V_{OH1}	Output High Voltage	0.85 V_{CC}		V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ Min
V_{OH2}		V_{CC} − 0.4			I_{OH} = −100 µA, $V_{CC} = V_{CC}$ Min
V_{ID}	A_9 intelligent Identifier™ Voltage	11.50	13.00	V	
I_{ID}	A_9 intelligent Identifier™ Current		500	µA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} during Read-Only Operations	0.00	V_{CC} + 2.0V	V	**NOTE:** Erase/Programs are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} during Read/Write Operations	11.40	12.60	V	

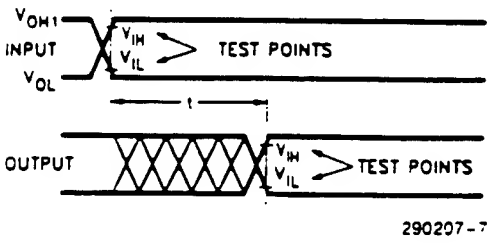
CAPACITANCE(3) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Limits		Unit	Conditions
		Min	Max		
C_{IN}	Address/Control Capacitance		6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

NOTES:
1. Active I_{CC} current of a typical device is 12 mA with nominal V_{CC} at room temperature.
2. Active I_{PP} current of a typical device is 10 mA with nominal V_{PP} at room temperature.
3. Sampled, not 100% tested.

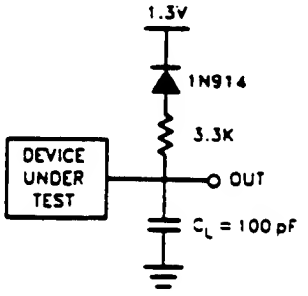
SAN040039

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at V_{OH1} for a logic "1" and V_{OL} for a logic "0". Testing measurements are made at V_{IH} for a logic "1" and V_{IL} for a logic "0". Rise/Fall time ≤ 10 ns.

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

A.C. TEST CONDITIONS

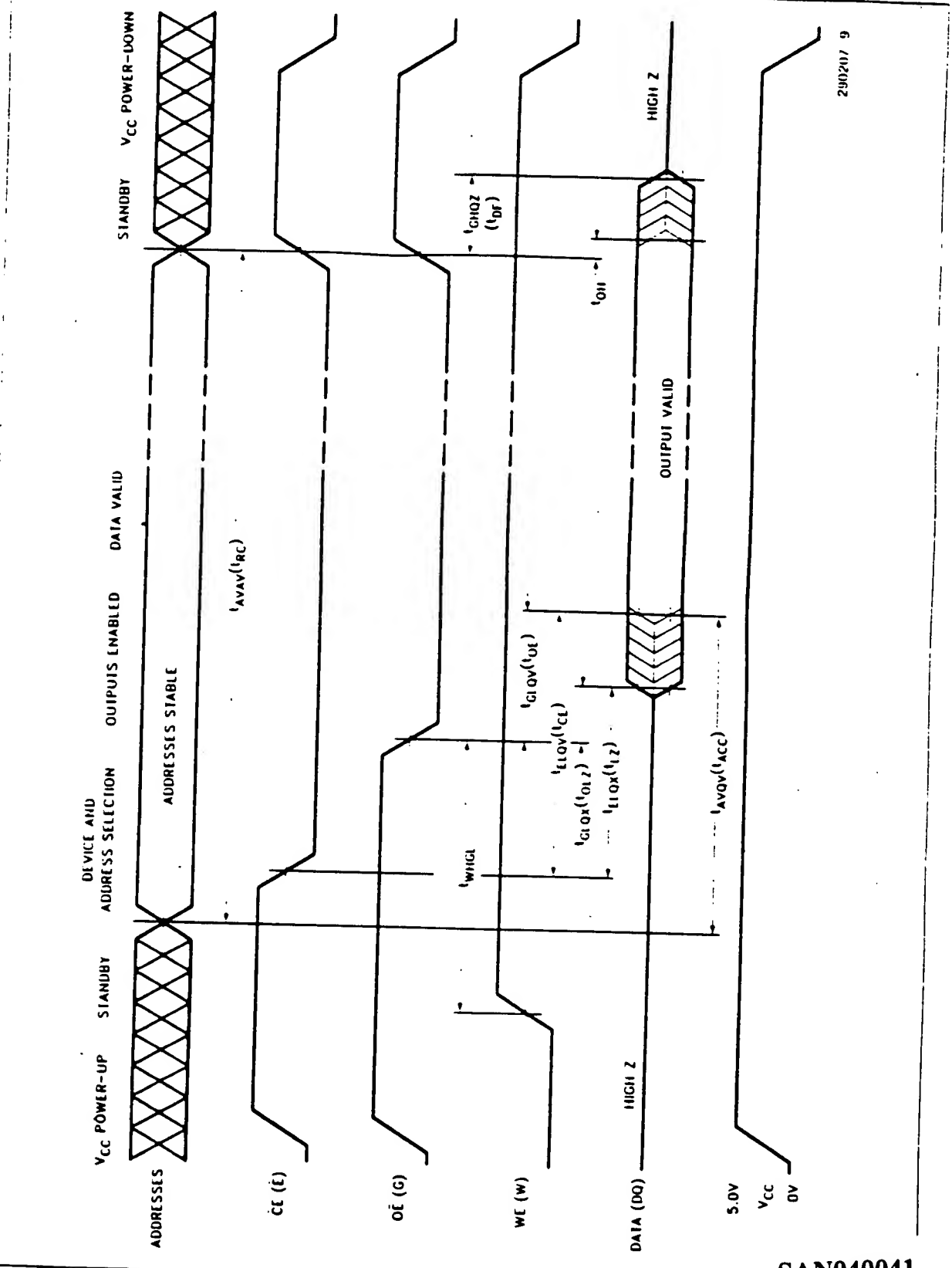
Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... V_{OL} and V_{OH1}
Input Timing Reference Level ..... V_{IL} and V_{IH}
Output Timing Reference Level ..... V_{IL} and V_{IH}

A.C. CHARACTERISTICS—Read-Only Operations

Versions		28F010-135P1C4		28F010-150P1C4		28F010-200P1C4		Unit
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time	135		150		200		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time		135		150		200	ns
t_{AVQV}/t_{ACC}	Address Access Time		135		150		200	ns
t_{GLQV}/t_{OE}	Output Enable Access Time		50		55		60	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	0		0		0		ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	0		0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z		30		35		40	ns
t_{OH}	Output Hold from Address, $\overline{CE}$, or $\overline{OE}$ Change(1)	0		0		0		ns
t_{WHGL}	Write Recovery Time before Read	6		6		6		μs

NOTES:
1. Whichever occurs first.
2. Rise/Fall Time ≤ 10 ns.

SAN040040



SAN040041

Figure 6. A.C. Waveforms for Read Operations

A.C. CHARACTERISTICS—Write/Erase/Program Operations(1)

Versions		28F010-135P1C4		28F010-150P1C4		28F010-200P1C4		Unit
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time	135		150		200		ns
t_{AVWL}/t_{AS}	Address Set-Up Time	0		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time	60		60		75		ns
t_{DVWH}/t_{DS}	Data Set-up Time	50		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time	10		10		10		ns
t_{WHGL}	Write Recovery Time before Read	6		6		6		µs
t_{GHWL}	Read Recovery Time before Write	0		0		0		µs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time before Write	20		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time	0		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width(2)	50		50		60		ns
t_{ELEH}	Alternative Write(2) Pulse Width	70		70		80		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High	20		20		20		ns
t_{WHWH1}	Duration of Programming Operation	10	25	10	25	10	25	µs
t_{WHWH2}	Duration of Erase Operation	9.5	10.5	9.5	10.5	9.5	10.5	ms
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low	100		100		100		ns

NOTES:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to A.C. Characteristics for Read-Only Operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (within a longer Write-Enable timing waveform) all set-up, hold, and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. Rise/Fall time ≤ 10 ns.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Chip Erase Time		0.5(1)	30	Sec	Excludes 00H Programming Prior to Erasure
Chip Program Time		2(1)	24(2)	Sec	Excludes System-Level Overhead
Erase/Program Cycles(3)	10,000	100,000		Cycles	

SAN040042

NOTES:
1. 25°C, 12.0V V_{PP}, 10,000 Cycles.
2. Minimum byte programming time excluding system overhead is 16 µsec (10 µsec program + 6 µsec write recovery), while maximum is 400 µsec/byte (16 µsec x 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Refer to RR-60 "ETOX™ Flash Memory Reliability Data Summary" for typical cycling data and failure rate calculations.

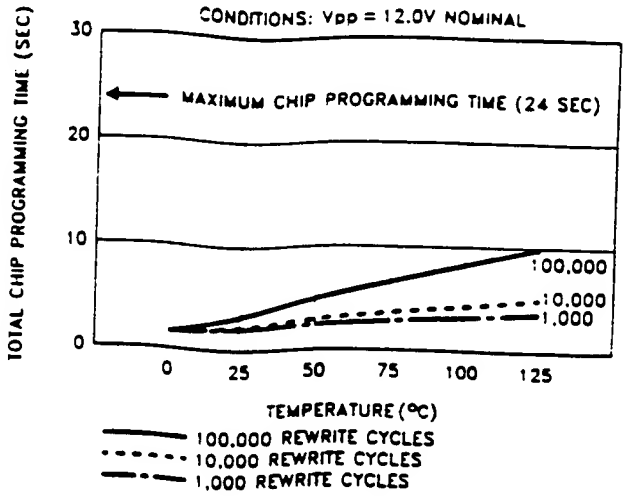


Figure 7. 28F010 Typical Programming Time vs. Temperature

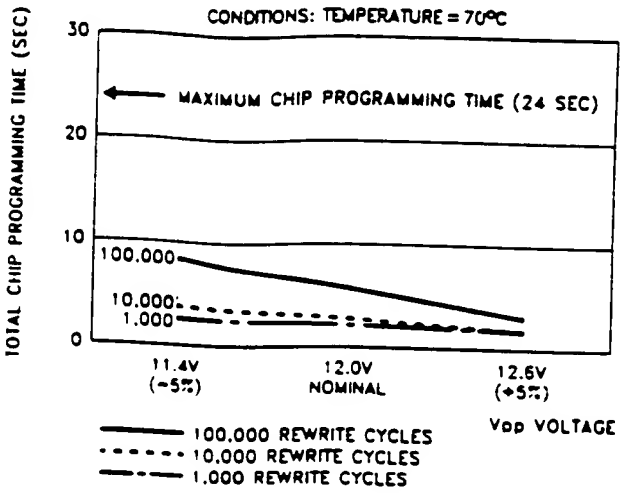


Figure 8. 28F010 Typical Programming Time vs. V_{PP} Voltage

SAN040043

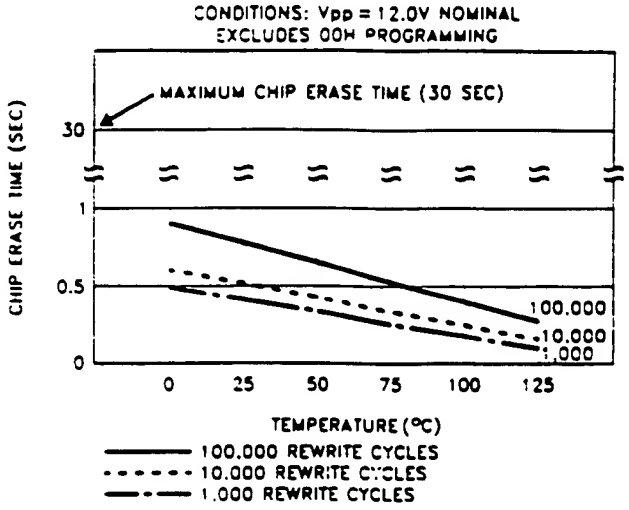


Figure 9. 28F010 Typical Erase Time vs. Temperature

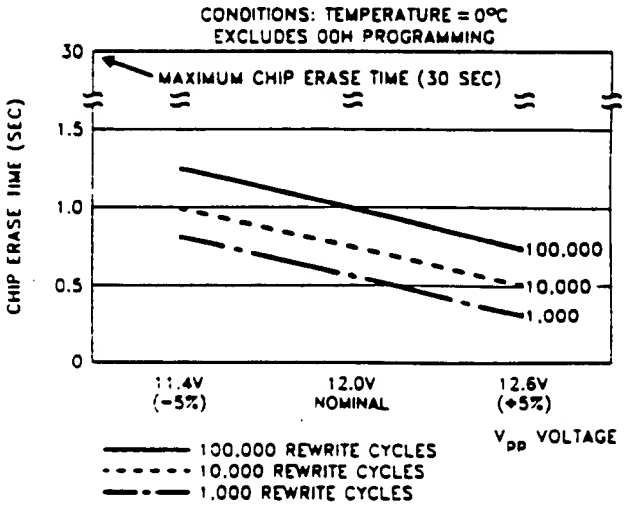


Figure 10. 28F010 Typical Erase Time vs. V_{PP} Voltage

SAN040044

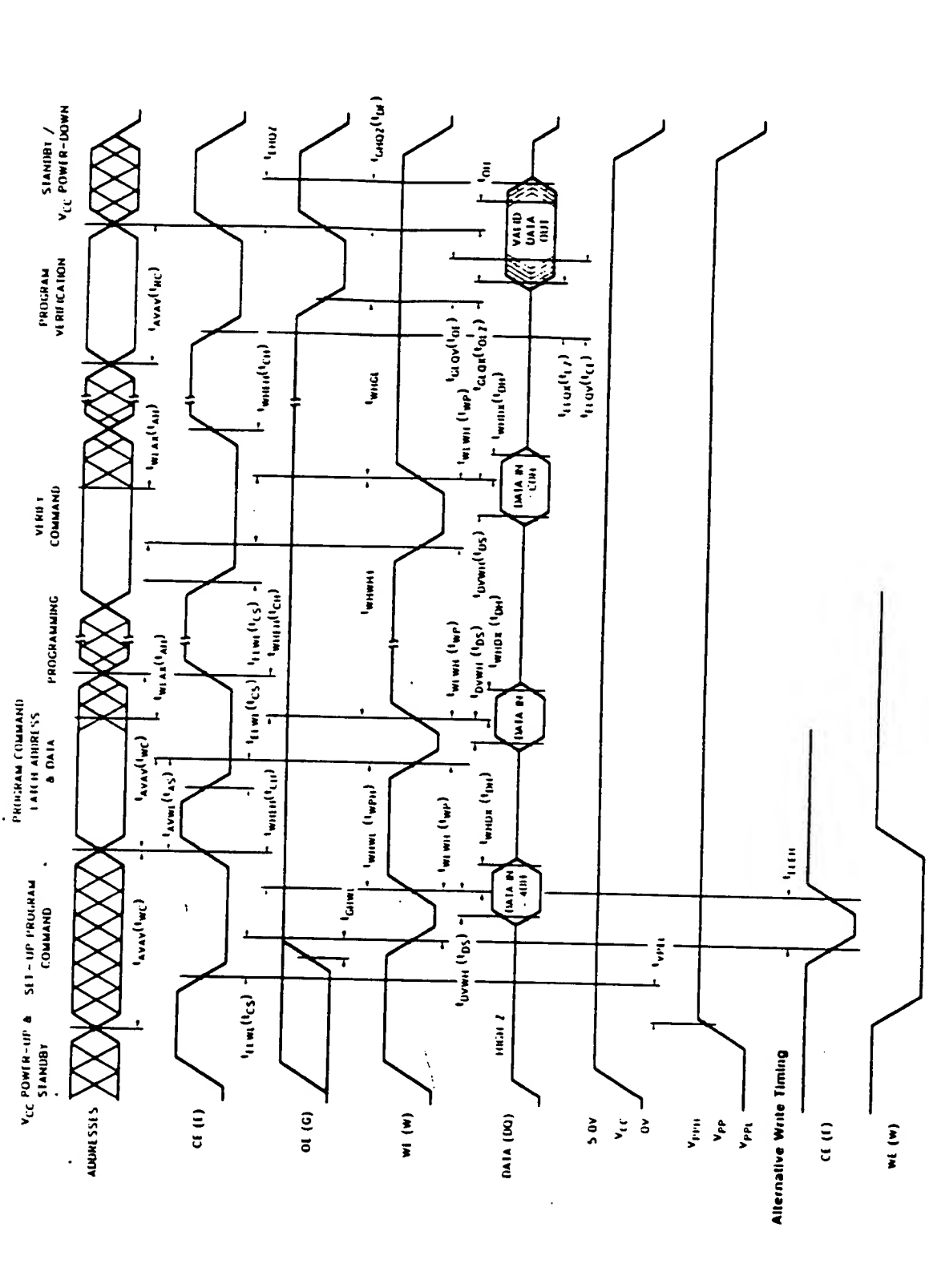


Figure 11. A.C. Waveforms for Programming Operations

SAN040045

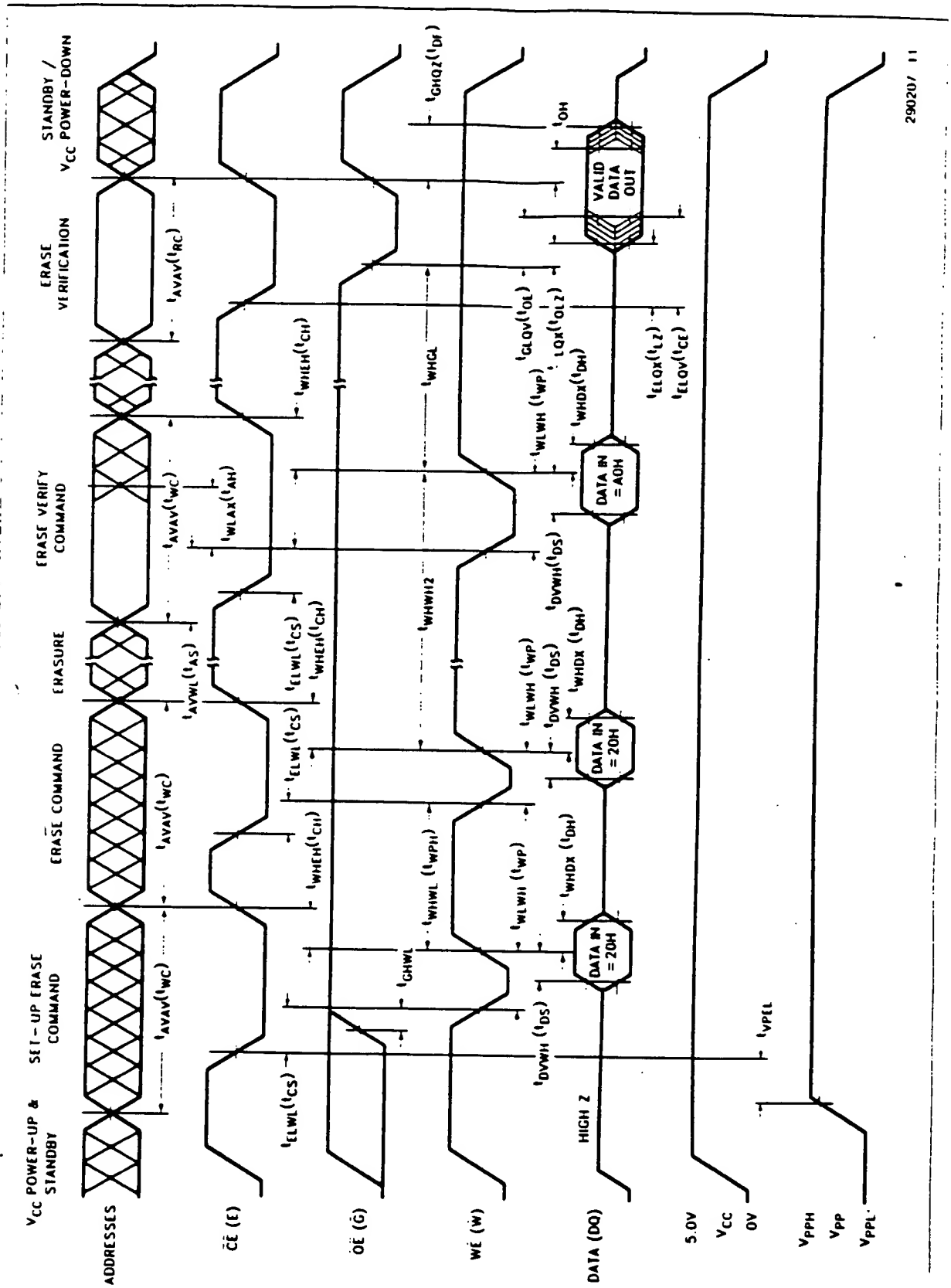
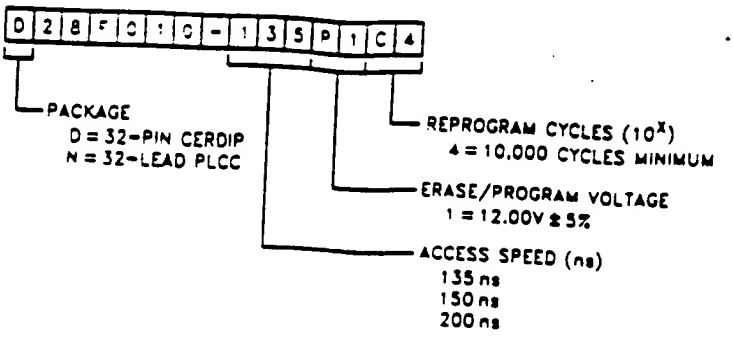


Figure 12. A.C. Waveforms for Erase Operations

SAN040046

Ordering Information



Valid Combinations:

D28F010-135P1C4	N28F010-135P1C4
D28F010-150P1C4	N28F010-150P1C4
D28F010-200P1C4	N28F010-200P1C4

ADDITIONAL INFORMATION

	Order Number
ER-20, "ETOX™ Flash Memory Technology"	294005
ER-24, "The Intel 28F010 Flash Memory"	294008
RR-60, "ETOX™ Flash Memory Reliability Data Summary"	293002
AP-316, "Using Flash Memory for In-System Reprogrammable Nonvolatile Storage"	292046

SAN040047

intel

ADVANCE INFORMATION

28F020
2048K (256K x 8) CMOS FLASH MEMORY

- Flash Electrical Chip-Erase
  - 2 Second Typical Chip-Erase
- Quick-Pulse Programming™ Algorithm
  - 10 µs Typical Byte-Program
  - 4 Second Chip-Program
- 10,000 Erase/Program Cycles Minimum
- 12.0V ±5% V_{PP}
- High-Performance Read
  - 150 ns Maximum Access Time
- CMOS Low Power Consumption
  - 30 mA Maximum Active Current
  - 100 µA Maximum Standby Current
- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- Noise Immunity Features
  - ±10% V_{CC} Tolerance
  - Maximum Latch-Up Immunity through EPI Processing
- ETOX™-II Flash-Memory Technology
  - EPROM-Compatible Process Base
  - High-Volume Manufacturing Experience
- Compatible with JEDEC-Standard Byte-Wide EPROM Pinout
  - 32-Pin DIP

(See Packaging Spec., Order # 231369)

Intel's 28F020 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F020 adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F020 increases memory flexibility, while contributing to time- and cost-savings.

The 28F020 is a 2048-kilobit nonvolatile memory organized as 262,144 bytes of 8 bits. Intel's 28F020 is offered in 32-pin cerdip or 32-lead PLCC packages. Pin assignments conform to JEDEC standards for byte-wide EPROMs.

Extended erase and program cycling capability is designed into Intel's ETOX-II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F020 performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming™ and Quick-Erase™ algorithms.

Intel's 28F020 employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 150 nanosecond access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 100 µA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from $-1V$ to $V_{CC} - 1V$.

With Intel's ETOX-II process base, the 28F020 levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

SAN040048

September 1989
Order Number: 290245-001

intel

ADVANCE INFORMATION

SM28F001
1 MBYTE (512K x 16) CMOS FLASH SIMM

- High-Performance
  - 135 ns Maximum Access Time
  - 14.81 MB/s Read Transfer Rate
- 100,000 Rewrite Cycles Typical/ Component
- Flash Electrical Chip-Erase
  - 1 Second Typical Chip-Erase
- 16 µs Typical Word Write
  - Up to 1 Mb/s Write Transfer Rate
- Inherent Non-volatility (Zero Retention Power)
  - No Batteries or Disk Required for Back-up
  - 800 µA Maximum Standby Current
- ETOX™ Flash-Memory Technology
  - High-Volume Manufacturing Experience
- JEDEC Standard 80-Pin Insertable Module
  - 0.050 Centerline Lead Spacing
  - Upgrade Path through 2 Gbytes
- Hardware Presence Detect
- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- Noise Immunity Features
  - ± 10% V_{CC} Tolerance
  - Maximum Latch-Up Immunity Through EPI Processing
- 12.0V ± 5% V_{PP}

Intel's 1 Mbyte flash SIMM (Single In-Line Memory Module) is the most cost-effective and reliable solution for read/write random access nonvolatile memory. The module offers higher performance, lower power, smaller form factor and weight than disk based medium, replacing DRAM and disk in many space constrained reprogrammable and embedded applications. The flash module is also ideal for high performance code and data storage as well as data accumulation. The 1 Mbyte flash SIMM is targeted for fixed and expandable, high density memory in space constrained applications. In addition, the module offers the inherent benefit of board space savings to those unable to take advantage of today's advanced, high density surface mount technology.

The 1 Mbyte Flash SIMM, composed of eight 1 Mb flash memories in plastic leaded chip carrier (N28F010), is organized as 524,288 words of 16 bits. The PLCCs are mounted, four to a side, together with 0.1 µF decoupling capacitors on an 80-pin JEDEC standard, low-profile module. The electrical characteristics of the module are very similar to the N28F010.

Intel's 1 Mbyte flash SIMM employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 135 ns access time provides no-WAIT state performance for a wide range of microprocessors and microcontrollers. Maximum standby current of 800 µA translates into power savings when the memory module is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from −1V to V_{CC} + 1V.

SAN040049

October 1989
Order Number: 290244-001

intel®

APPLICATION NOTE

AP-316

October 1989

Using Flash Memory for In-System Reprogrammable Nonvolatile Storage

SAUL ZALES
DALE ELBERT
APPLICATIONS ENGINEERING
INTEL CORPORATION

SAN040050

Order Number: 292046-002

1.0 INTRODUCTION

Intel's ETOX™ II (EPROM tunnel oxide) flash memory technology uses a single-transistor cell to provide in-system reprogrammable nonvolatile storage. Reprogramming entails electrically erasing all bits in parallel and then randomly programming any byte in the array. This new technology offers designers alternatives for two of industry's needs: 1) a cost-effective means of updating program code; and 2) a solid-state approach for non-volatile data accumulation or storage.

This application note:

- introduces you to the concepts of in-system writing;
- discusses the hardware and software considerations for reprogramming flash memories in-system;
- offers a checklist for integrating Intel's flash memories into microprocessor- or microcontroller-based systems; and
- shows an example of an 80C186 design which incorporates flash memory.

1.1 PROM Programmer vs System-Processor Controlled Programming

While soldered to a printed circuit board, one of two sources controls flash memory reprogramming: 1) a PROM programmer connected to the board, or 2) the system's own central processing unit (CPU). These are called on-board programming (OBP), and in-system writing (ISW), respectively. With OBP, the PROM programmer supplies the programming voltage (V_{PP}) and the programming intelligence; with ISW, V_{PP} is generated locally and the system itself drives the reprogramming process. Both methods offer a variety of benefits. However this application note focuses on ISW.

NOTE:
See Appendix A for OPB design considerations.

1.2 Information Download and Upload

ETOX II flash memory technology programs extremely quick, permitting "on-the-fly" programming with unbuffered 19.2K baud data input. The remote ISW system handles the serial communication link for the host interface, as well as the flash memory reprogramming.

Version Updates (Download)

Flash memories enable code version updates using simple hardware designs. Beyond the basic system, a local V_{PP} supply is all that is needed for remote code download.

A central host computer can download program code to many remote systems. Flash memory offers this capability without the drawbacks of other technologies. It is solid-state and nonvolatile, thus eliminating mechanical component wear-out (common with disk drives) and the risk of losing updates (a concern with battery-backed RAM). These aspects of flash memory offer major advantages in automated factories, remote systems, portable equipment and other applications. Finally, flash memories provide this capability at a much lower cost than byte-alterable EEPROM and battery-backed SRAM.

Data Acquisition (Upload)

Intel's flash memories allow single-byte programming for data accumulation applications. A remote data-logger uploads its information to a central host via serial link. The flash memory device is then in-system erased

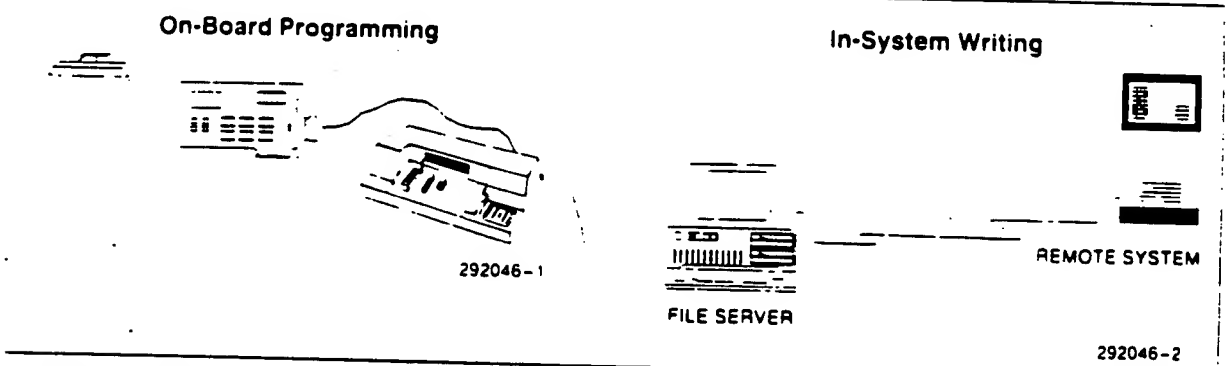


Figure 1. These diagrams illustrate OBP and ISW. In OBP, a PROM programmer updates a system's flash memory. The ISW diagram shows a host updating remote flash memory via serial link. The remote system performs the flash reprogramming with its own CPU.

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for resumption of data acquisition. This is useful in an advanced electrical power meter, for example. It could be configured to track and monitor power usage and report the data to a central computer for billing and utility management. This reduces the cost of manual door-to-door meter reading.

2.0 DEVICE FEATURES AND ISW APPLICATION CONSIDERATIONS

This section gives a brief overview of Intel's flash memory features and explains how they facilitate ISW design.

2.1 Flash Memory Pinouts

The 32-pin DIP memory site is forward-compatible from the 256K bit to the 2 Mbit flash memory density. It fits into the 27C010 Mbit EPROM pinout and requires no multiplexed pins. Also, with just a single circuit-board jumper trace, a 28-pin EPROM can be placed in the lower pins of the 32-pin flash memory site. (See Figure 2. Flash Memory Pinouts.) For more information on intertechnology pin compatibility see Ap Bnef AB-25.

Byte-Wide Flash Memory in 32-Pin DIP

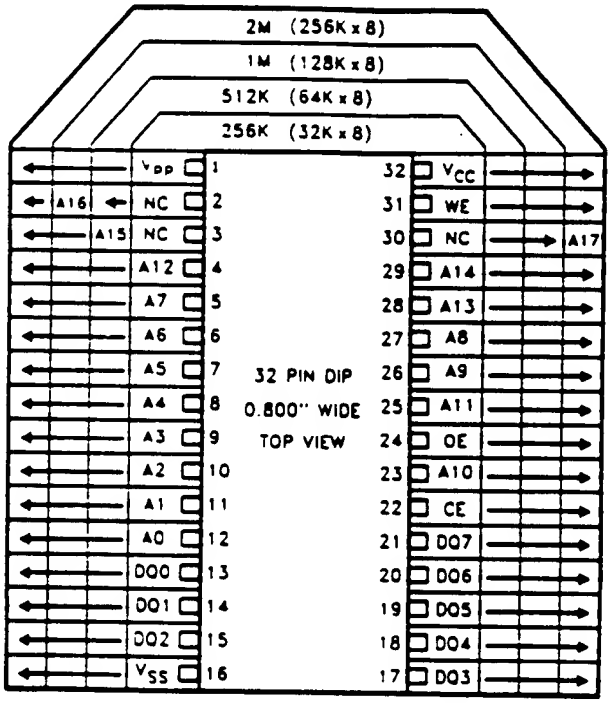

Figure 2. Flash Memory Pinouts

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Byte-Wide Flash Memory in 32-Pin PLCC

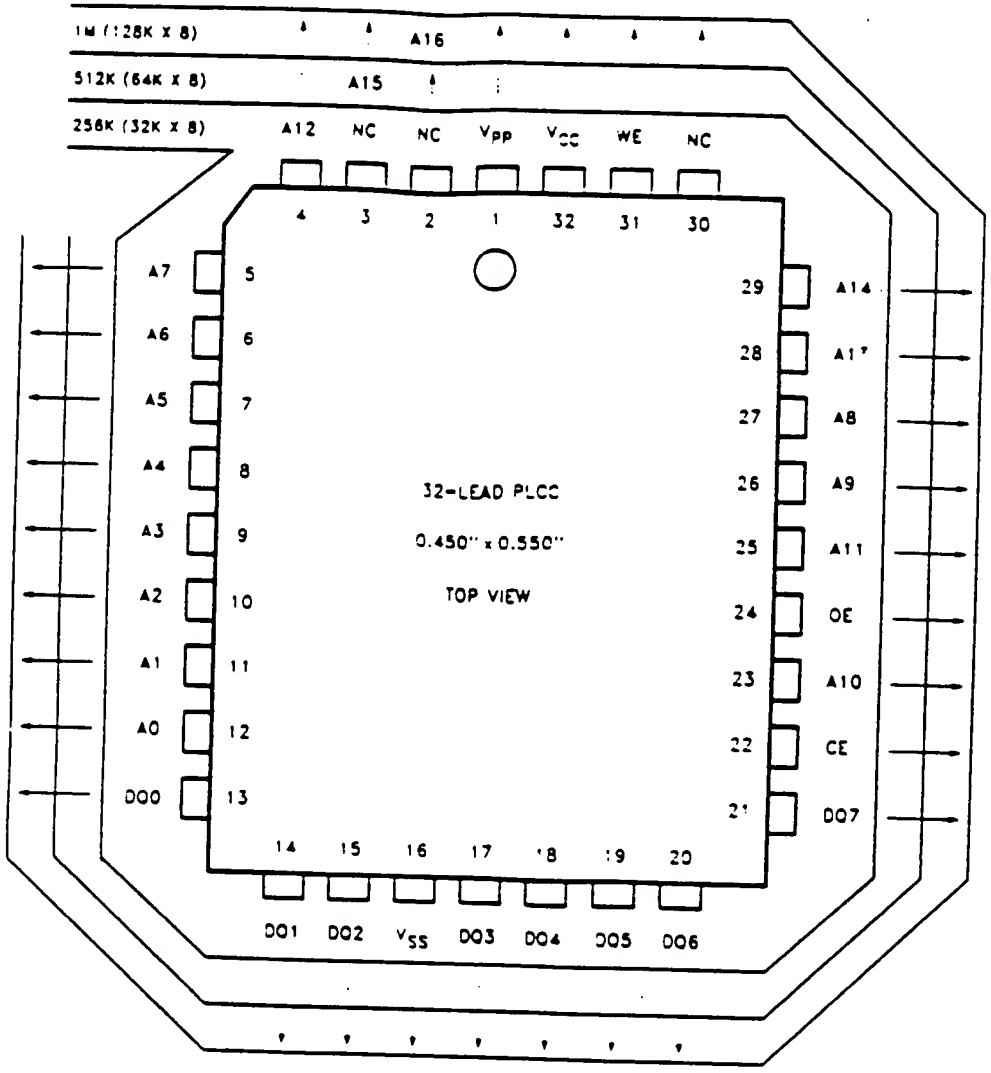

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Figure 2. Flash Memory Pinouts (Continued)

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Table 1. Command Register Instructions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation	Addr(1)	Data(2)	Operation	Addr(1)	Data(2)
Read Memory(3)	1	Write	X	00H	Read	Valid	Valid
Read Inteligent Identifier™	1	Write	X	90H	Read	00/01H	ID
Set-Up Erase/Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Set-Up Program/Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset(3)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Addresses are latched on the falling edge of the Write-Enable pulse.
EA = Address of memory location to be read during erase verify.
PA = Address of memory location to be read during program verify.
2. EVD = Data read from location EA during erase verify.
PD = Data to be programmed at location PA. Data is latched on the rising edge of Write-Enable.
PVD = Data read from location PA during program verify. PA is latched on the Program command.
3. The second bus cycle must be followed by the next desired command register write, given the proper delay times.

2.2 Command Register Architecture

Simplified Processor Interface

Intel's command register architecture simplifies the processor interface. The command register allows CE\, WE\, and OE\ to have standard read/write functionality. All commands such as "Set-up Program" or "Program Verify" can be written with standard system timings. Raising V_{PP} to 12V enables the command register for memory read/write operation, while lowering V_{PP} below V_{CC} − 2V restores the device to a read only memory.

Writing to the register toggles an internal state-machine. The state-machine output controls device functionality. Some commands require one write cycle, while others require two. The command register itself does not occupy an addressable memory location. The register simply stores the command, along with address and data needed to execute the command. With this architecture, the device expects the first write cycle to be a command and does not corrupt data at the specified address. Table 1 contains a list of command register instructions.

The following sections describe the commands in relation to device operation. For more information on the command register see the appropriate flash memory data sheets, and Section 4.4 "Reprogramming Routines".

Read Memory Command—00H

This command allows for normal memory read operations with V_{PP} turned on. After writing the command and waiting 6 µs, the CPU can read from the memory at system speeds. Once placed in the read mode no further action is required on the command register.

Read Inteligent Identifier™ Command—90H

Most PROM programmers read the device's Inteligent Identifier to select the proper programming algorithm. On EPROMs, raising A9 to the V_{PP} level configures the device for this purpose. Since this is unacceptable in-system, you can read the flash memory Inteligent Identifier by first writing command 90H. Follow this by reading address 0000 and 0001H for the manufacturer and device ID. Reset the device with the Read Memory command after you have read the identifier.

Set-Up Erase/Erase Commands—20H

Write this command (20H) twice in succession to initiate erasure. The first write cycle sets up the device for erasure. The device starts erasing itself on the second command's rising edge of Write-Enable. You must stop erasure by issuing the Erase Verify command.

NOTE:
Prior to erasure, it is necessary to program all bytes to the same level (data = 00H). See the Quick-Erase™ algorithm for more details.

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Erase Verify Command—A0H

The erase command erases all bytes of the array in parallel. After each erase operation, all bytes must be verified to see if they erased. Write the Erase Verify command (A0H) to stop erasure and set-up verification.

The device latches the address to be verified on the falling edge of WE\ and the actual command on the rising edge. Wait 6 μs before reading the data at the address specified on the previous write cycle.

The flash memory applies an internally-generated reference voltage to the addressed byte. Reading 0FFH from the addressed byte in this mode indicates that all bits in the byte are erased with sufficient margin to V_{CC} and temperature fluctuations.

If the location is erased, then repeat the Erase Verify procedure for the next address location. Write the command prior to each byte verification to latch the byte's address. Continue this process for each byte in the array until a byte does not return 0FFH data, or the last address is accessed.

In the case where the data read is not 0FFH, perform another erase operation. (Refer to Set-up Erase/Erase). Continue verifying from the address of the last verified byte. Once you have accessed the last address, erasure is complete and you can proceed to program the device. Terminate the erase verify operation by writing another valid command (e.g., Program Set-up).

Set-up Program/Program Commands—40H

Write this command (40H) twice in succession to initiate programming. The first write cycle sets up the device for programming. The device latches address and data on the falling and rising edges of the second write cycle, respectively. It also begins programming on the rising edge. You stop the programming operation by issuing the Program Verify command.

Program Verify Command—C0H

Flash memory devices program on a byte-by-byte basis. After each programming operation, the byte just programmed must be verified. Write the Program Verify command (C0H) to stop programming and set-up verification. The device executes this command on the rising edge of Write-Enable. The program Verify command stages the device for verification of the byte last programmed. No new address information is latched.

The flash memory applies an internally-generated reference voltage to the addressed byte. Wait 6 μs before reading the data at the address programmed. Reading valid data indicates that the byte programmed successfully.

Command Register Reset—FFH

Flash memories reset to the read mode during power-up, and remain in this mode as long as V_{PP} is less than V_{CC} + 2V. If your system leaves V_{PP} turned-on during a *system reset*, then incorporate a command register *device reset* into the hardware initialization routines. This is necessary because the CPU might be controlling programming or erasure when the system reset hits. Reset the flash memory early in the boot routine to minimize potential over-programming or over-erasure.

Write the reset command (0FFH) twice in succession to reset the device. The double write is necessary because of the state-machine reprogramming structure. For example, suppose the *system* is reset after a Set-up Program command. The flash memory state machine expects the next write cycle to contain valid address and data for programming, followed by another write cycle for program verification. The first Reset command will be mistaken for program data but will not corrupt the existing data. This is because the command (data = 0FFH) is a null condition for flash memory programming. Only data bits programmed to zero pull charge onto the memory cell and change the data. The second write cycle actually resets the device to the read function. Following the second reset cycle, you can write the next command (Read, Program Set-up, Erase Set-up, etc.).

If the V_{PP} supply is turned off upon system reset, the software reset is not required. The flash memory will reset itself automatically when V_{PP} powers down.

Data Protection on Power Transitions

The command register architecture offers another benefit in addition to simplified processor interface—during system power-up and power-down it protects data from corruption by unstable logic. Erasure or programming require V_{PP} to be greater than V_{CC} + 2V and the proper command sequence to be initiated. For example the CPU must write the erase command twice in succession. The odds of this occurring randomly are slim. For even greater security, you can switch V_{PP} as discussed in Section 3.13.

2.3 V_{PP} Specifications

Flash memories, like EPROMs, require a 12V externally-generated power supply for reprogramming. Intel's V_{PP} specifications 12.0V ±0.6V (5%) is compatible with most off-the-shelf (or available in-system) power supplies. (Note, Section 3.1 discusses V_{PP} generation techniques, and Appendix B shows different circuit alternatives.)

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It is essential to use the specified V_{PP} when reprogramming the flash memory device. Once the command to erase, program, or verify is issued, the device internally generates the required voltages from the V_{PP} supply. The command register controls selection of internal reference circuitry tapped off of V_{PP}. An improper V_{PP} level causes the references to be wrong, degrading the performance of the part.

(When programming U.V. EPROMs, V_{CC} is raised to 6.5V. On flash memories, the V_{PP} reference circuitry and command register architecture provide the same function while keeping V_{CC} and V_{PP} at static levels. An incorrect V_{CC} level during U.V. EPROM programming poses similar hazards to improper V_{PP} levels on flash memories.)

The hardware design section discusses various methods for generating V_{PP}.

3.0 HARDWARE DESIGN FOR ISW

Covered in this section are the following:

- Description of ISW-specific functional system blocks including memory requirements
- V_{PP} generation techniques
- Communication Considerations

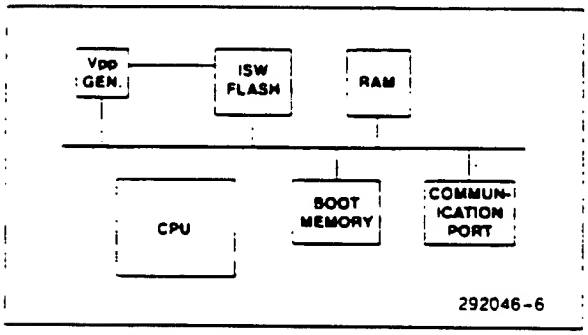

Figure 3. System Block Diagram

System Level Hardware Requirements for ISW:

- processor or controller
- limited amount EP/ROM or other flash memory devices for boot code, communications s/w, and reprogramming algorithms
- limited amount of RAM for variable storage (i.e., stacks, buffers, and other changing parameters)
- communications capability
- flash memory for nonvolatile code or data storage needs
- V_{PP} generator or regulator

All of the functional blocks in Figure 3 are typical of any embedded or reprogrammable system with the exception of the V_{PP} generator. Some microcontrollers have on-chip EP/ROM, RAM and a serial port. With these devices, implementation of the ISW capability requires little additional hardware.

The next section discusses V_{PP} generation techniques and communications design considerations.

3.1 V_{PP} Generation

A static V_{PP} is needed to reprogram flash memories. The V_{PP} voltage can be generated by:

1) regulating it down from a higher voltage;
2) pumping it up from a lower voltage (i.e., charge pump, DC/DC converter, etc.); or
3) designing or specifying the system's 12V supply with the required ISW tolerances and specifications.

Sufficient current for reprogramming should be considered when selecting your V_{PP} generation option. Parallel reprogramming for flash memory in 16-bit or 32-bit systems will require, respectively, 2X or 4X additional current capability.

3.1.1 REGULATING DOWN FROM HIGHER VOLTAGE

V_{PP} is obtained from a higher voltage by using a linear regulator. Given the higher voltage, regulation offers the least expensive method of generating V_{PP}. Standard three terminal 12V $\pm 1\%$, $\pm 2\%$, $\pm 4\%$ non-adjustable regulators are available off-the-shelf. Some regulators have on/off control built-in. (See Appendix B, V_{PP} Circuit #1.) All regulators require a minimum input voltage greater than the output voltage. (See Appendix B, V_{PP} Circuit #2 and #3.)

3.1.2 PUMPING 5V UP TO 12V

V_{PP} can be obtained by pumping V_{CC} and regulating it to the proper voltage. A voltage charge-pump can be designed and built by using a charge-pump integrated circuit and some discrete components (see Appendix B, V_{PP} Circuit #4 and #5) or by using a monolithic DC/DC converter (see Appendix A, V_{PP} Circuit #6).

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When using adjustable circuits containing discrete components, design the output voltage so it falls within the V_{PP} specifications for all corners of the components' skew (i.e., $V_{CC} \pm 10\%$; $Rx \pm 1\%$, $Ry \pm 1\%$, etc.). Include the resistors' temperature coefficients in the calculation matrix. Note that each of the various components can add error to the V_{PP} supply.

The monolithic DC/DC converter shown in Appendix B Circuit #6 fits into a 24-pin socket. It offers the advantages of close temperature tracking and ease of implementation. It has also been characterized at temperatures and meets all the V_{PP} specifications. Appendix C contains a partial list of vendors selling DC/DC converters.

Most DC/DC converters are only 50–60% efficient, so heat dissipation may be a concern. Some discrete boost circuits such as Appendix B, Circuit #5, offer much higher efficiency (70-85%).

In all V_{PP} generation methods, a capacitor on the input voltage terminals reduces the output noise voltage. Some power supplies (Appendix B, Circuits #3 and #4) specify a large-valued capacitor to decrease the Effective Series Resistance (ESR). Place a 0.1 μF capacitor within 0.25 inches of each flash memory's V_{PP} input (in addition the one on the V_{PP} generator's input).

NOTE:
The ESR is inversely proportional to the capacitance value and the rated working voltage. To lower the ESR choose a capacitor with a large capacitance and a high working voltage (i.e., above 100V).

3.1.3 ABSOLUTE DATA PROTECTION—V_{PP} ON/OFF CONTROL

With V_{PP} below $V_{CC} - 2V$, internal circuitry disables the command register and eliminates the possibility of inadvertent erasure or programming. Switching the V_{PP} supply off provides the secondary benefits of improved power and thermal management.

There are two ways to switch V_{PP} on and off

1) directly switch the V_{PP} generator's output, or
2) switch the input voltage supplying the regulation circuit.

Any switching circuit will cause a voltage drop, so choose a switch with this drop in mind. Some power supplies have asymmetrical tolerances on 12V (i.e. -5%, -4%). Flash memory allows the 12V supply to drop as low as -5%. The 1% difference between the supply and the device requirement allows the switch to have an ON resistance voltage drop of 0.12V. Continuing with this example, assume the system only reprograms one flash memory at a time. The current through the switch into the flash is $I_{PP} = 30$ mA. Solving for the allowable resistance across the switch: $R = V/I = (0.12V)/(30\text{ mA}) = 4$ Ohms. See Figure 4, Example Voltage Drop Across Switch.

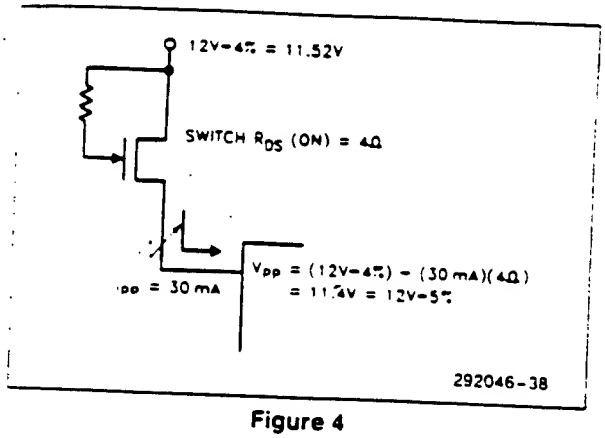

Figure 4

Controlling the input voltage of a DC/DC convertor with a MOSPOWER FET is a straightforward approach. (See Appendix B, Circuit #6.) Choose the FET switch carefully. It should have a very low on-resistance to minimize the voltage divider effect of the converter and FET switch. If the voltage across the FET switch is too high, the converter will not have the proper input voltage to meet its specifications. Always design the switching circuit with sufficient margin to maximum V_{PP} and V_{CC} load currents.

3.1.4 WRITES AND READS DURING V_{PP} TRANSITIONS

After switching V_{PP} off, the CPU can read from the flash memory without waiting for the capacitors on V_{PP} to bleed off. To do this, write the Read Memory command prior to issuing the V_{PP}_OFF instruction. Alternatively, the device resets automatically to read mode when V_{PP} drops below $V_{CC} - 2V$.

Raising V_{PP} to 12V enables the command register. You must wait 100 ns after V_{PP} achieves its steady state value before writing to the command register. Remember that the steady state V_{PP} settling time depends on both the power supply slew rate and the capacitive load on the V_{PP} bus.

3.1.5 OTHER V_{PP} CONSIDERATIONS

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The V_{PP} pin is an MOS input which can be damaged by electrostatic discharge (ESD). In OBP applications, an external power source supplies V_{PP} and then is removed. Electrostatic charge can build up on the floating V_{PP} pin. You can solve this problem by one of two means: 1) tie the pin to V_{CC} through a diode and pull-up resistor (Figure 5a) or through a resistor to ground (Figure 5b). With either approach use a 10 KΩ resistor to minimize V_{PP} power consumption.

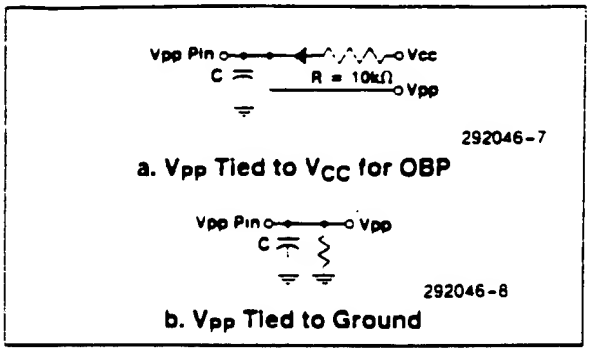

Figure 5

NOTE:
Typically EPROMs require V_{PP} to be within one diode drop of V_{CC} for optimal standby power consumption. Either approach can be used with the flash memory.

ISW applications do not require this ESD protection as most regulators and charge pumps contain a voltage divider on the output stage. A divider provides a resistive path to ground even with the supply turned off. (Note: check the schematics of the V_{PP} supply chosen.) However, if you directly switch the V_{PP} supply, add the resistor to ground; the switch isolates the V_{PP} pin and allows charge to build up.

3.1.6 V_{PP} CIRCUITRY AND TRACE LAYOUT

You should lay out V_{PP} circuitry and traces for high frequency operation since programming power characteristics exhibit an AC current component. Use the following standard power supply design rules:

- Keep leads as short as possible and use a single ground point or ground plane (a ground plane eliminates problems).
- Locate the resistor network (or a regulator) as close as possible to the adjustment pin to minimize noise pick-up in the feedback loop. The resistor divider network should also be as short as possible to minimize line loss.
- Keep all high current loops to a minimum length using copper connections that are as wide as possible. (This will decrease the inductive impedance which otherwise causes noise spikes.)
- Place the voltage regulator as close to the flash memory as practical to avoid an output ground loop. Excessive lead length results in an error voltage across the distributed line resistance.
- Separate the input capacitor return from the regulator load return line. This eliminates an input ground loop, which could result in excessive output ripple.

3.2 Communications—Getting Data to and from the Flash Memory

The flash memory does not care about the origin of the data to be programmed. The data could be downloaded from a serial link, parallel link, disk drive, or generated locally as in data accumulation applications.

While most systems communicate via serial link, sending a font to a printer's flash memory is an example of a parallel interface. In either format, designers must decide whether or not to buffer the incoming data. Error-free serial protocols will require buffering for reconstruction of information packets. With equal capacity of RAM ar flash memory in a system, the download time would only be limited by the speed of the communication link.

Both worst case and typical analysis must be done for real time download and un-buffered programming. The maximum transmission rate is 19.2K baud assuming worst case programming times. The time between characters at 19.2K baud is 520 µs; the worst case byte programming time is approximately 0.5 ms (including software overhead). Typical byte programming takes 16 µs which allows for much higher unbuffered transmission rates. However, a single byte can take up to the full 400 µs specified time (plus software overhead), so you should not base transmission rate on typical programming times.

Partial buffering or FIFO schemes can also be implemented to increase transmission rates. An argument for buffering is reduction of interconnect time and costs.

4.0 SOFTWARE DESIGN FOR ISW

Covered in this section are the following software requirements:

- system integration of ISW
- reprogramming considerations for single- and multiple-flash memory based designs.

4.1 System Integration—Boot Code Requirements

Boot code in remote systems should contain various ISW-specific procedures in addition to standard initialization and diagnostic routines.

The most dependable boot code for remote version updates contains some basic communications capability and the ISW reprogramming algorithms. Thus, a data-link disruption while reprogramming would be recoverable. For manufacturing flexibility, this boot memory could be an OBP 256K flash memory.

1. Bootstrap, and reset flash memory;
2. Check "HOST_INT" and "VALID_AP" flags:

   If HOST_INT is inactive and VALID_AP = 4150H, jump to application start address;
3. If VALID_AP < > 4150H, loop and wait for host (the link probably went down during update);
4. When "HOST_INT" is active, vector to host interaction code.

   (See next section.)

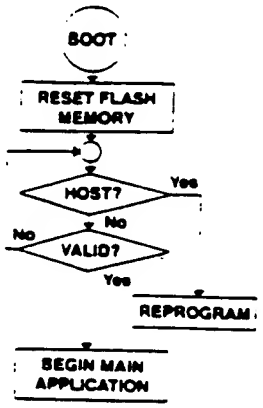

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Figure 6. Example of ISW Integration to the Boot Sequence

An alternative to storing these routines in a separate boot device is storing them in the flash memory containing the program code. Prior to erasure, the CPU would transfer the ISW routines to system RAM and execute from there. This type of approach is suitable for systems with back-up power supplies.

The communication link could be disrupted during reprogramming, leaving the device in an unknown configuration. Therefore, the boot code should reset the flash memory and check two ISW flags. The following section discusses the flag check concept.

4.1.1 ISW FLAG CHECK

After resetting the flash memories and initializing other system components, the CPU should check the communications link for a host interrupt. We will call this the HOST_INT flag. Had the communication link gone down prior to completion of downloading, then the host would have to re-establish contact to complete the task.

Assuming no HOST_INT request has been made, the boot protocol then checks a data sequence in the flash memory signifying a valid application (VALID_AP). You program this sequence into the memory array after confirmation of a successful download. If a download is interrupted midway through erasure or programming, then the VALID_AP flag locations will not contain the VALID_AP code. On the next system bootstrap the CPU recognizes this and holds up system boot until valid code is programmed. In Figure 6 an example flag protocol uses the VALID_AP sequence of 4150H (ASCII codes for "AP").

4.2 Communication Protocols and Flash Memory ISW

The remote download communications protocol must guarantee accurate transmission of flash memory instructions and program code. This protocol can be as simple as a read-back technique or as complex as an error-free transmission protocol. (See Figure 7 for possible system-level flash memory instructions.)

A simple read-back technique optimizes download for boot code memory needs and ease of implementation. The embedded CPU echoes the flash memory instruction (i.e., Erase or Program) to the host, and waits for a confirmation prior to execution. After programming the update, the remote system checks the update by transmitting it back to the host for confirmation. The remote system then programs the VALID_AP sequence. Note that programming and reading back 64 Kbytes at 19.2K baud takes about 0.57 minutes per direction:

(65,536 bytes) * (10 bits/byte) * (1 sec/19.2 Kbits) * (1 min/60 sec) = 0.57 minutes.

Implementing either software- or hardware-based error-free communications protocol improves transmission efficiency. It eliminates the possibility of errant data being programmed if not buffered and checked, and optimizes the download process for transmission time. Additionally, file compression and decompression routines can improve the transmission rate.

General ISW instructions include:
- STATUS CHECK
- INITIATE REPROGRAMMING
- MOVE ISW ROUTINES FROM FLASH MEMORY TO RAM (If not resident in separate boot memory)

Data accumulation-specific commands include:
- RETRIEVE DATA
- ERASE FLASH MEMORY

Figure 7. Sample System-Level ISW Instruction Set

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Status Check

The host should request a status update from the remote system prior to sending a reprogramming instruction. Depending on the response, the host may break the link and reconnect later, or it may send an erasure or data-upload command. This type of handshaking is necessary when system downtime for reprogramming might not be acceptable. An example of this is an automated factory where robots handle caustic chemicals.

4.3 Data Accumulation Software Techniques

Data can be accumulated in a remote environment with flash memory and then uploaded to a host computer for manipulation. You can adapt various standard data-logging techniques for use with flash memory. With any technique, you determine the next available memory location by reading for erased data (0FFH). This address would only be located once on system bootstrap and then recalled from RAM and incremented as needed.

Given a repeating data string of known length and composition, program start and stop codes at either end of the string. Do not pick 00H or 0FFH data for these codes because they are used during erasure. The start and stop codes enable the CPU to differentiate between available memory for logging and logged data equal to 00H or 0FFH.

For non-regular data input, you can address this same issue by programming the logged data followed by the variable identifier. Again, do not pick 00H or 0FFH data for the variable identifiers.

With any technique, the host computer separates and manipulates the data after the uploading operation.

4.4 Reprogramming Routines

Intel's ETOX flash memories provide a cost-effective updatable, non-volatile code storage medium. The reliability and operation of the device is based on the use of specified erasure and programming algorithms.

Intel offers reprogramming software drivers to make it easy for you to design and implement flash memory applications. The software is designed around the CPU-family architectures and requires minimal modification to define your system parameters. For example, you supply the memory width (8-bit, 16-bit, or 32-bit), system timing, and a subroutine for control of V_{PP}.

NOTE:
Contact your nearest sales office for details.

If you prefer to implement the algorithms yourself, they are outlined in the device data sheets. Command register instructions required for the various operations are included in the data sheet flow charts.

The following sections describe both single-device and multiple-device parallel reprogramming implementations.

4.4.1 Quick-Erase™ Algorithm

Flash memories chip-erase all bits in the array in parallel. The erase time depends on the V_{PP} voltage level (11.4V–12.6V), temperature, and number of erase/write cycles on the part. See the device data sheets for specific parametric influences on reprogramming times.

Note that prior to erasing a flash memory device the processor must program all locations to 00H. This equalizes the charge on all memory cells insuring uniform and reliable erasure.

Algorithm Timing Delays

The Quick-Erase algorithm has three different time delays:

1) The first is an assumed delay when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on V_{PP}, the delay required is proportional to the number of flash memory devices times 0.1 µF/device. V_{PP} must reach its final value 100 ns before the CPU writes to the command register. Systems that hardwire V_{PP} to the device can eliminate this delay.
2) The second delay is the "Time Out TEW" function, where TEW is the erase timing width. The function occurs after writing the erase command (the second time) and before writing the erase-verify command. The erase-verify command internally stops erasure. To insure proper device operation, the CPU must issue this command, or the device will continue to erase until the memory cells are driven into depletion. Should this happen the internal decode circuitry will no longer select unique addresses. A symptom of this condition (over-erasure) is an error when the CPU attempts to program the next time. One can occasionally recover over-erased devices by programming all addresses with data = 00H.

   TEW for ETOX II flash memories is 10 ms ± 500 µs. This delay can be either software or hardware controlled. Either way, the timing tolerance allows for interrupt-driven timeout routines. It is the responsibility of the designer to insure a high interrupt-priority to the timer such that response latency is within 500 µs allowed for TEW.
3) The third delay in the erase algorithm is a 6 µs time out between writing the erase verify command and reading for 0FFH. During this delay, the internal voltages of the memory array are changing from the

erase levels to the verify levels. A read attempt prior to waiting 6 µs will give false data—it will appear that the chip does not erase. Repeatedly trying to erase verify the device without waiting 6 µs will cause over-erasure. This delay is short enough that it is best handled with software timing.

High Performance Parallel Device Erasure

In applications containing more than one flash memory, you can erase each device serially or you can reduce total erase time by implementing a parallel erase algorithm.[7] You save time by erasing all devices at the same time. However, since flash memories may erase at different rates, you must verify each device separately. This can be done in a word-wise fashion with the command register Reset command and a special masking algorithm.

Take for example the case of two-device (parallel) erasure. The CPU first writes the data word erase command 2020h twice in succession. This starts erasure. After 10 ms, the CPU writes the data word verify command A0A0h to stop erasure and setup erase verification. If both bytes are erased at the given address, then the CPU increments the address (by 2) and then writes the verify command A0A0h again. If neither byte is erased, then the CPU issues the erase sequence again without incrementing the address.

Suppose at the given address only the low byte verifies FFh data? Could the whole chip be erased? The answer is yes. Rather than check the rest of the low byte addresses independently of the high byte, simply use the reset command to mask the low byte from erasure and erase verification on the next erase loop. In this example the erase command would be 20FFh and the verify command would be A0FFh. Once the high byte verifies at that address, the CPU modifies the command back to the default 2020h and A0A0h, increments the address by 2, and writes the verify command to the next address.

See Figure 8 for a conceptual view of the parallel erase flow chart and Appendix D for the detailed version. These flow charts are for 16-bit systems and can be expanded for 32-bit designs.

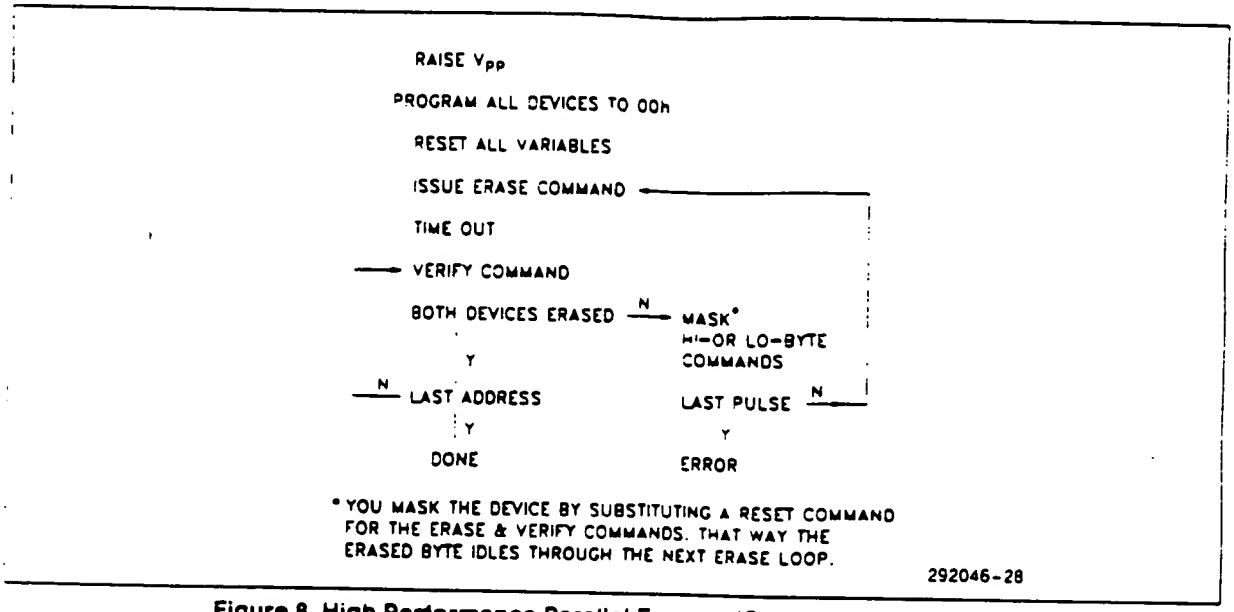

Figure 8. High Performance Parallel Erasure (Conceptual Overview)

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[7] Parallel Erasure and Programming require appropriate choice of V_{PP} supply to support the increased power consumption.

4.4.2 Quick-Pulse Programming™ Algorithm

Flash memories program with a modified version of the Quick-Pulse Programming algorithm used for U.V. EPROMs. It is an optimized closed-loop flow consisting of 10 µs program pulses followed by byte verification. Most bytes verify after the first pulse, although some may require more passes through the pulse/verify loop. As with U.V. EPROMs, this algorithm guarantees a minimum of ten years data retention. See the device data sheets for more details on the programming algorithm.

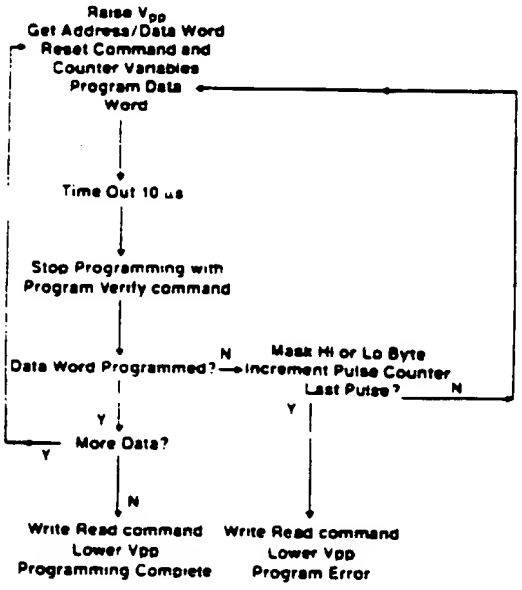
Algorithm Timing Delays

The Quick-Pulse Programming algorithm has three different time delays:

- The first and third—V_{PP} set-up and verify set-up delays—are the same as discussed in the erasure section. In this case the third delay is for the transition between writing the Program Verify command and reading for valid data.
- The second delay is the "Time Out 10 µs" function, which occurs after writing the data and before writing the program-verify command. This write command internally stops programming. It is essential to issue the command, or the device will continue to program until told to stop. The section entitled "Pulse Width Timing Techniques" gives 86-family assembly code for generating a 10 µs timer routine.

High Performance Parallel Device Programming

Software for word- or double-word programming can be written in two different manners. The first method offers simplicity of design and minimizes software overhead by using a byte programming routine on each device independently. Here you increment the address by 2 or 4 when addressing 1 of 2 or 4 devices, respectively. The second method offers higher performance by programming the word or double-word data in parallel. This method manipulates the command register instructions for independent byte control. See Figure 9 for conceptual 2-device parallel programming flow chart and Appendix E for the detailed version.



*You mask the device by substituting a Reset command for the Program and Verify commands. That way, the programmed bytes do not get further programmed on subsequent pulses.

Figure 9. Parallel Programming Flow Chart (Conceptual Overview)

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NOTE:
Word or double-word programming assumes 2 or 4 8-bit flash memory devices.

Parallel Programming Algorithm Summary:

- Decreases programming time by programming 2 flash memories (16 bits) in parallel. The algorithm can be expanded for 32-bit systems.
- Eliminates tracking of high/low byte addresses and respective number of program pulses by directing the CPU to write data-words (16-bit) to the command register.
- Maintains word write and word read operations. Should a byte on one device program prior to a byte on the other, the CPU continues to write word-commands to both devices. However, it deselects the verified byte with software commands. An alternative is to independently program high and low bytes using hardware select capability.

4.4.3 Pulse Width Timing Techniques

Software or hardware methods can be used to generate the timing required for erasure and programming. With either method you should use an in-circuit emulator (ICE™) and an oscilloscope to verify proper timing. Also remove the flash memory device from the system during initial algorithm testing. Incorrect timing can not only shorten the flash memory's life, but it can also affect system operation and reliability.

Software Methods and Examples

Software loops are easily constructed using a number of techniques. Timing loops need to be done in assembly language so that the number of clock cycles can be obtained from the instructions.

In order to calculate a delay loop three things are needed—

1) processor clock speed,
2) clock cycles per instruction, and
3) the duration of the delay loop.

As an example, the 80C186 divides the input clock by 2. With a 20 MHz input clock the processor's internal clock runs at 10 MHz. This translates to a 100 ns cycle time. Delays can be made by loading the CX register with a count and using the LOOP instruction. The LOOP instruction takes 16 clock cycles to execute per pass. It decrements the CX register on each pass and jumps to the specified operand until CX equals zero.

When writing a delay loop consider all instructions between the start and end of the delay. If a macro is written that delays 10 µs, add the clock cycles for all instructions in the macro.

Here is an example of a 10 µs delay and the calculation of the constant required for a 10 MHz 80C186.

```
WAIT_10 µs:
        push cs          :10 clock cycles
        mov cx,DELAY     :4 clock cycles
        loop $           :see looping time
        pop cx           :10 clock cycles

looping time = (15*[DELAY - 1] ÷ 5) clock
cycles
DELAY = ((10 µs/cycle time) - 24)/looping
time = 6
```

Hardware Methods

Using an Internal Timer—

Many microcontrollers and some microprocessors have on-chip timers. At higher input clock speeds these internal timers have a resolution of 1 µs or better. The timers are loaded with a count and then enabled. The timer starts counting and when it reaches the terminal count a bit is set. The CPU executes a polling algorithm that checks the timer status. Alternatively, a timer-controlled interrupt can be used. After the timer has been set and the interrupt enabled, the CPU can be programmed to wait in idle mode or it could continue executing until the timed interrupt.

One thing to take into account when using interrupts is the time required for the CPU to recognize and interrupt request (interrupt latency). This is important when figuring the timer value, because the time seen by the part will be the programmed delay plus the minimum interrupt latency time.

The 80C186 has three 16-bit timers on-chip. Timer #2 can be a prescaler for the other two timers, which extends timers #0 and #1 range out to 2^32. By using two timers, 10 μs pulses and 10 ms pulses can be easily achieved.

Using an External Timer—

External timers can take many forms. One popular example is the 82C54 (CHMOS Programmable Interval Timer) which has three 16-bit timers on-chip. One timer can be used as a prescaler for the others so that a count of 2^32 can be achieved as with the 80C186 internal timers.

5.0 SYSTEM DESIGN EXAMPLE: AN 80C186 DESIGN

A general purpose controller and/or data acquisition system was built to demonstrate 86-based ISW. The 80C186 CPU drives the system, which contains 16 Kbytes of EPROM (two 27C64's), 64 Kbytes of flash memory (two 28F256's), 64 Kbytes of SRAM (two 32K x 8's) three 8-bit ports (82C55A), one serial port (82510), and a 5V to 12.0V DC/DC converter. Three 74HC573's demultiplex the address/data bus and latch the byte high enable line (BHE) and the status lines (if needed). Two data transceivers (74HC245) simulate the worst case data path for a system requiring added drive capability. If the transceivers are not needed they can be replaced with wired headers. See Appendix F for detailed schematics parts list, and changes for the 28F512 or 28F010.

The 80C186 reset (output) drives the reset input on the 82510, 82C55A, and the OE\ inputs on the address latches and data transceivers. The reset line goes inactive 5 clock cycles before the first code fetch. Also, the CPU's write signal is split into byte-write-high and byte-write-low to allow for byte or word writes.

The 80C186 has on-chip memory and peripheral chip selects. Two of the memory chip selects are dedicated. One is the Upper Chip Select (UCS, dedicated for the boot area) and the second is the Lower Chip Select (LCS, for the interrupt vector table area). See the memory map in Figure 10.

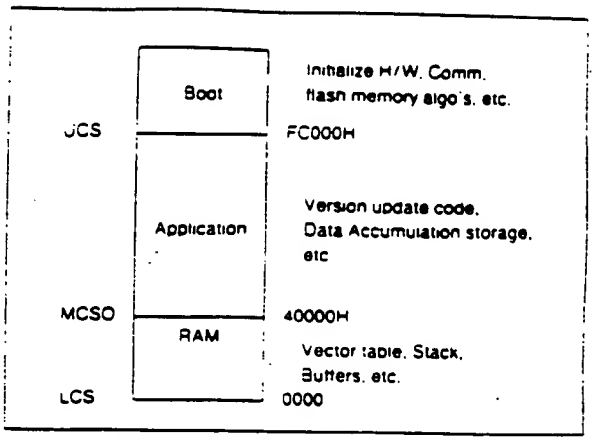

Figure 10. 80C186 Memory Map

The permanent code was placed in an EPROM in the UCS memory segment: this code includes routines for hardware initialization, communications, data uploading and downloading, erasure and programming algorithms, I/O drivers, ASCII to binary conversion tables, etc. This would be useful for systems reconfigured for different communication protocols as the last step prior to shipment.

Code and constants that might change are placed in the 64 Kbytes of flash memory. Application examples include operating systems, code for rapidly advancing biomedical technologies such as blood test software, engine-control code and parameters, character fonts for printers, postage rates, etc. The RAM is used for the interrupt table, stack, variable data storage, and buffers.

The three 8-bit ports on the 82C55A peripheral controller can be used for control and/or data acquisition. It powers-up with all port pins high. Similarly, all port pins go high after warm resets as well. Because the pins are high after a power-up/reset, an open collector invertor was used to control the MOSPOWER switch which in turn controls V_{PP}. You must drive the FET switch to one rail or the other to guarantee its low on-resistance. V_{PP} is turned off during power-up or reset as a hardware write protection solution. The DC/DC converter supplies V_{PP}.

The 82510 is a flexible single channel CHMOS UART offering high integration. The device off-loads the system and CPU of many tasks associated with asynchronous serial communications.

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The part can be used as a basic serial port for the host serial link, or can be configured to support high speed modem applications. For more information on the 82510 see the 82510 data sheet and AP-401 "Designing with the 82510 Asynchronous Serial Controller".

Software was written to download code and data parameters (code updates) from a PC to the demo board through the PC's COM1 port (serial port). The system also can upload data (remote data acquisition) to the PC via the same link.

Once the download code and data has been programmed it can not be lost, even if power should fail. This is because Intel's ETOX flash memory technology is based on EPROM technology and does not need power to retain data.

The end result: rugged, solid state, low power nonvolatile storage.

6.0 SUMMARY

Intel's flash memories offer designers cost-effective alternatives for remote version updates or for reliable data accumulation in the field or factory. Designers will also benefit from time savings in any kind of code development—no 15 minute waits for U.V. EPROM erasure.

This application note covers the basics of in-system writing to flash memories and can be used as a check list for systems other than the 80C186 design shown. The basic concepts remain the same: a CPU controls the reprogramming operations; a 12V supply must be applied to the flash memory for erasure and programming; and a communications link connects the host to the remote system and supplies the code to be programmed.

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APPENDIX A
ON-BOARD PROGRAMMING DESIGN CONSIDERATIONS

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INTRODUCTION

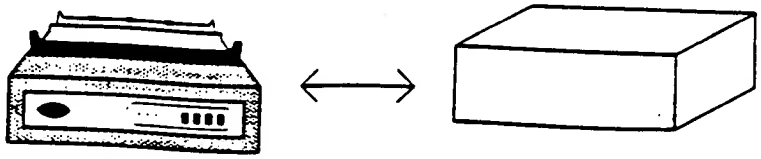
On-board programming[1] (OBP) with Intel's flash memory provides designers with cost reduction capabilities for alterable code storage designs. When used in conjunction with on-board programming, flash memory presents opportunities for savings in two areas: greater testability in the factory, which translates to improved outgoing quality and reduced return rate; and quicker, more reliable field updates, which translates to decreased product support cost.

This appendix:

- outlines the design considerations associated with on-board programming, and the improvements afforded by Intel's flash memory;
- offers guidelines for converting current 64K EPROM OBP designs;
- designs an 8-bit system for on-board programming;
- suggests some 16-bit flash design considerations; and offers information on OBP equipment and vendors.

[1] With on-board programming, non-volatile memory is programmed while socketed or soldered on the application board, rather than before hand as a discrete component. This programming method is also called in-module or in-circuit programming, and has been practiced by some major corporations since 1981. See sidebar on following pages for more information on U.V. EPROM OBP usage.

HOST APPLICATION (Printer Shown Here) **BOARD-PROGRAMMER**



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On-Board Programming Manufacturing Example—A printer is customized via OBP for international markets: 1. printer assembly completed, diagnostics code programmed and tested, and unit stored in inventory; 2. order arrives for printer with foreign language font; 3. diagnostics code flash-erased, and desired font programmed; 4. printer ships to customer.

INTEL'S FLASH MEMORY—DESIGNED TO MEET YOUR OBP NEEDS

Intel's flash memory simplifies OBP code updates by offering designers the command register architecture. As described in section 2.2, this architecture offers the full reliability of EPROM off-board programming without the hassles of elevating V_{CC}.

5 Volt Vcc Erasure and Programming Verification

Unlike EPROM OBP, flash memory enables Vcc to remain at 5.0V throughout all operations. Internal circuitry derives the erasure and programming verification levels from the voltage on Vpp rather than from Vcc. These verify modes enable use of a single Vcc bus for the entire board, as opposed to the two buses needed for U.V. EPROM OBP. (See sidebar entitled EPROM OBP).

EPROM OBP

EPROM OBP has been a proven manufacturing technique since 1981. Ingenuity and clever circuit design have enabled manufacturers to overcome the hurdles associated with OBP and enjoy the benefits.

In many cases, Intel's flash memory simplifies today's solutions and offers new capabilities to advance the state of OBP technology. The following paragraphs outline the hurdles and a few of the solutions in use today.

EPROMs require program verification at an elevated V_{CC} to insure long-term data retention. PROM programmers easily accommodate this requirement, and it is generally invisible to the end-user.

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REPLACING CURRENT EPROM OBP DESIGNS WITH FLASH MEMORY

Hardware Considerations

A slight hardware modification is required to adapt most of the current EPROM OBP designs for use with Intel's flash memory. Simply convert the EPROM memory sites from 28 to 32 pins. All other board-design criteria used for EPROM OBP apply to flash memory as well. (For discussions of these criteria see section entitled New OBP Designs).

A standard EPROM OBP requires the board designer to bus $\overline{PGM}$ to the edge connector. With flash memories' command register architecture, this same trace enables electrical erasure and programming, only now the line is called Write Enable ($\overline{WE}$). The timing for $\overline{WE}$ is similar to that of read accesses, although that is handled via software changes.

Another potential hardware change is on the board programmer side of the design—the V_{PP} supply. Many EPROMs program with 12.5-13.0V V_{PP} supplies. Intel's ETOX II flash memory requires 11.4-12.6V V_{PP}. This change should not be an issue since the V_{PP} supply on many board programmers is programmable.

Mixed memory systems containing both conventional U.V. EPROM and flash memories require special consideration. This type of memory design requires separation of the Chip Enable ($\overline{CE}$) control lines between the EPROM and flash devices to allow for independent programming control and access. The $\overline{PGM}$ and $\overline{WE}$ lines can be common if the board programmer can give the appropriate timings to either type of device.

Software Considerations

Manufacturers who program EPROMs on-board today will need new board-programmer software to take advantage of flash memory's feature set, specifically software for the Quick-Erase™ and Quick-Pulse Programming™ algorithms.

Benefits of Converting Your EPROM OBP Design to Flash

The most pressing reason to convert from a standard EPROM to flash memory is the total cost savings. To appreciate this, you must consider your way of doing business at the board and system levels—from the factory to installation and repair in the field. In the factory, boards can be tested with a diagnostics program in the flash memory and then erased and reconfigured for shipment in the same step. Improved testing will decrease the probability of field failures and costly customer returns. Simplified test and rework methods will decrease your inventory holding costs. Also, if in the process of converting to flash memory you include the ability to OBP via a cable-connector, service calls for code updates will be quicker, more reliable, and cost less money. Your serviceman would simply connect the programming equipment to the system without dismantling it to remove the EPROMs. (See section entitled The System/Board-Programmer H/W Connection for details.)

EPROM OBP (cont'd)

With OBP, the EPROM board-programmer handles the elevated-V_{CC} requirement easily as well. However, when V_{CC} is greater than 5V, logic devices populating the same board may draw excessive current and not operate predictably.

One solution to this issue involves running separate V_{CC} traces to the board's edge connector—one for EPROM programming, and one for powering up the rest of the board.

A second consideration when designing for EPROM OBP has been accessing manufacturer and device codes.

The identifier mode requires forcing A9 to 12V. This translates to adding extra isolation, which implies the increased costs of buffers and extra board space.

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NEW OBP DESIGNS

Design Considerations

As with EPROM in-circuit programming, flash memory board programming requires the use of a board-programmer. Unlike U.V. erasure for standard EPROM OBP, electrical erasure enables flash memory OBP without removing the board from the system.

We will look at designing a board that is to remain powered-up in the system during erasure and reprogramming. The key concept is to design the board in such a way that the programmer can take control of the system during code updates. The implementation of such a design is straightforward, easy, and suited to automated production assembly.

Taking Control

The board-programmer needs to take control of the system's address bus, data bus, control lines, etc. to update the code without damaging the system. (See Figure 2, System to Board-Programmer Interface.) Taking control simply means isolating the rest of the system from these lines.

Various methods of isolating the memory from the system include using tristate buffers, latches, or even the capabilities designed into microprocessors (μP) and microcontrollers (μC). For example, Intel's 86-based μP family has HLD/HLDA signals that were set-up for multiprocessor system designs where bus control is a major concern. The HLD signal, when acknowledged, tristates the address, data, and control lines. Although not designed for multiprocessor environments, Intel's MCS®-51 and MCS-96 microcontroller families have Reset capabilities to help simplify this same task.

One issue to be aware of when using a CPU's reset control function is that it may switch from the reset to active condition at a non-standard logic level. This only presents a problem if the address/data buffer takes longer to activate than the CPU, and the CPU attempts to fetch code from a memory device isolated from it.

One approach to insure successful programming takeover (i.e. without bus contention) is to have the board-programmer's lines in a high impedance state during connection to the system. Once connection to the system has been secured, the serviceman could hit a button on the board-programmer to start the system takeover procedure. Then when total control has been established, the programmer would commence with erasure and reprogramming.

Aside from the flash device's isolation from the system, various CPU control lines ($\overline{MEMRD}$, $\overline{WE}$, $\overline{PSEN}$, etc.) may need isolation as well. If active during Reset, these lines may put the CPU into an unspecified state. When designing a board for OBP, check the μC/μP data sheets carefully for any special reset conditions.

Printed Circuit Board Guidelines for V_{CC} and V_{PP}

Programming conventional EPROM and flash memories takes 30 mA of current on V_{CC} and V_{PP}, due to the nature of hot-electron injection. Most of the charge transfers to the memory cell's floating gate in a short current spike during the first pulse. You should design both the V_{CC} and V_{PP} traces with A.C. current spikes in mind. Wherever possible, limit the inductance by widening the two traces. Bypass capacitors (0.1 μF) should be placed as close as possible to the memory device's V_{CC} and GND pins, as well as the devices V_{PP} and GND pins. The capacitor on V_{CC} decreases the power supply droop. The capacitor on V_{PP} supplies added charge, and filters and protects the memory from high frequency over-voltage spikes[2].

2. For a complete discussion of electrical noise, grounds, power supply distribution and decoupling see AP-74—High Speed Memory System Design Using the 2147H, and AP-125—Designing Microcontroller Systems for Electrically Noisy Environments.

EPROM OBP (cont'd)

Some users of OBP get around this issue by programming all EPROMs with a common algorithm. However, this practice compromises the device's reliability, and should not be done.

A better solution than ignoring the identifier is to choose a qualified EPROM vendor and program with its algorithm only.

One subtle concern with EPROM OBP that designers often overlook is U.V. board erasure.

→ U.V. EPROM board erasure requires removal of the board from its host system. This incurs the hidden costs of labor, lower yields due to handling, and the reliability risks of dismantling a system. Flash memory decreases these costs by enabling a greater degree of factory automation, and increases the flexibility afforded by OBP.

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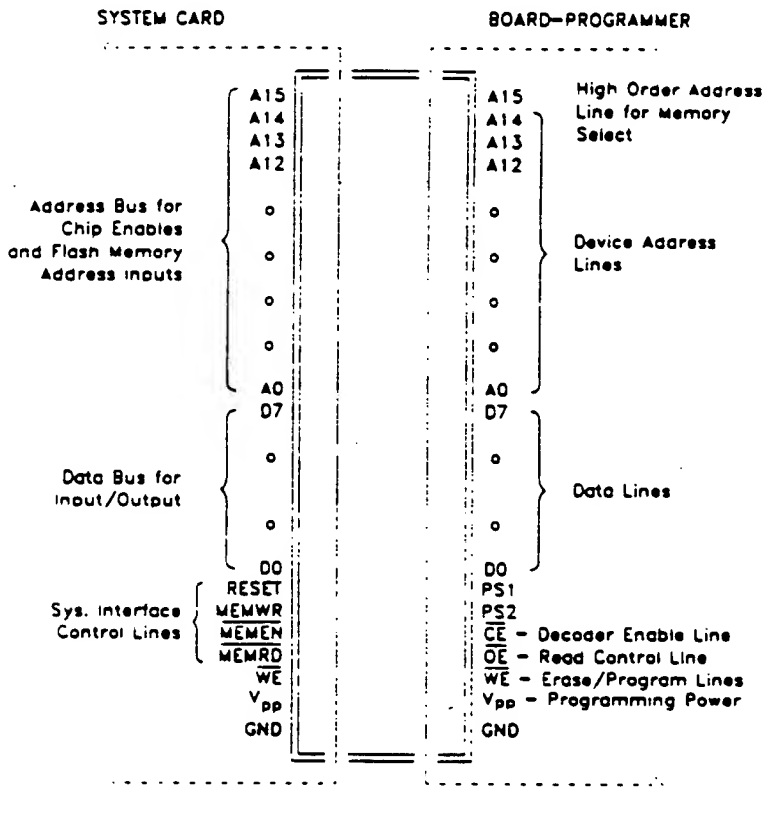


NOTE:
During normal system read operation, all interface traces are left open-circuited. Some of the lines have pull-downs or weak pull-ups to insure proper device operation.

Figure 2. System to Board-Programmer Interface

EPROM OBP (cont'd)

→ Special U.V. board erasers must be purchased, at significant costs and with limited throughput. A low-end U.V. bulb costs $75-$100 each. A U.V. board eraser system could cost upwards of $10,000, with recurring costs of light bulbs and energy. Thus, the cost of U.V. erasure is often under-estimated.

→ Although portable board programmers are commercially available, U.V. lights by nature are not very rugged, and are not suited for out-of-factory code updates. This complicates field service.

→ Erasure can be easily controlled in a lab environment; however, it is not as clear on the manufacturing floor which label to remove for U.V. erasure, because parts other than EPROMs have windows (i.e. EPLD's, micro-controllers with embedded EPROM memory, etc.)

SAN040070

The System/Board-Programmer Hardware Connection

In most U.V. EPROM OBP applications, designers use the board's edge-connector as the programmer interface. This approach is the lowest cost solution for standard EPROM technology because U.V. erasable devices require system disassembly for erasure anyway. With flash memory, you can eliminate the system dismantling and capitalize on the erase feature by adding a cable connector to the board for reprogramming purposes. The connector should extend from the board through the system's chassis, and should be easy to reach by a serviceman.

Various types of cables exist on the market that could be used to connect programming equipment to the system. The key design consideration when choosing the type of cable is elimination of all transient noise that would interfere with the programming or erasure process.

Three types of noise interference and methods to diminish the noise are as follows:

1. line to line cross-talk (due to board-programmer's drivers that drive sharp step functions on adjacent address lines): solved with either ribbon cables, having alternate lines grounded, or with braided twisted-pairs that have a ground line for each active signal;
2. programmer line-driver-to-board impedance mismatches leading to transmission line effects of signal reflection, and interference: solved by limiting cable length, decreasing programmer switching speed (or allowing longer settling time between address switches) or by using matched line drivers on the programmer and high impedance buffers on the board end, or by using series termination resistors on the driving end of the cable (i.e.—board-programmer end, with the exception of the bi-directional data bus which needs series resistors at both ends);
3. rf pick-up in electrically noisy environments: use either shielded cable such as coax, ribbon cable with solid copper ground plane, or a new type that has recently become available called Flex cable.

Braided twisted-pair cables when kept under three feet in length generally reduce cross-talk to acceptable levels. This type of cable offers the most cost-effective solution which works well in most applications. Depending on the environment, the programmer and your design, you may need a combination of solutions, such as braided twisted-pairs with series termination.

At first all of these alternatives may seem expensive or superfluous, but keep in mind that the cost of a single cable and programmer gets amortized over the total number of systems programmed.

AN 8-BIT BUS DESIGN EXAMPLE

An example of an in-circuit reprogrammable controller board is an 80C31, two 28F256's and some glue chips. (See Figure 3. for a system block diagram. See Appendix A. for a detailed system schematic.)[3] The important issues for erasure and reprogramming are as follows:

1. the board-programmer must have uncontested access and control of the flash memory array; and
2. the microcontroller must be reset (un-active) during the erasure and programming cycles.

SYSTEM DESIGN

Bus Control Circuitry

The 80C31 has an active-high reset pin, which tristates the address and data bases. Route this line (RESET) to the programming connector. Tie the $\overline{OE}$ pins on the low-order address latch (74HCT573), and the $\overline{PSEN}$ buffer-enable (74HCT125)[4] together, and route that line MEMWR[5] to another pin on the programmer-interface connector.

During normal system operations when the µC reads program code from the 28F256 devices, the pull-down on MEMWR keeps the address latches and $\overline{PSEN}$ buffer active. During flash memory OBP, the board-programmer drives MEMWR active-high, which disables these outputs, and isolates the address bus and $\overline{PSEN}$ from the programming signals.

The board-programmer must independently control the RESET and MEMWR traces because they disable at different V_{IL} values (2.5V for RESET vs 0.8V for MEMWR). If controlled by the same 5V supply, on power-up or after a reset condition the µC would try to execute code while still isolated from its code source—specifically before the address latches and $\overline{PSEN}$ buffer activate.

Address Decode Circuitry

This design shows two 28F256 flash memories. Systems with more than one memory device typically decode the CPU's high-order address to select a particular device.

3. Note that the flow-through latch on the data bus is not needed with the 80C31, but is drawn as an example for CPU's that can not tristate their data bus.
4. The isolation buffer is required on $\overline{PSEN}$ in this design because the 80C31 goes into unspecified states when the Reset and $\overline{PSEN}$ lines are active simultaneously. To avoid any possible problems, buffer $\overline{PSEN}$.
5. MEMWR = > bus isolation control of $\overline{PSEN}$ and the data bus.

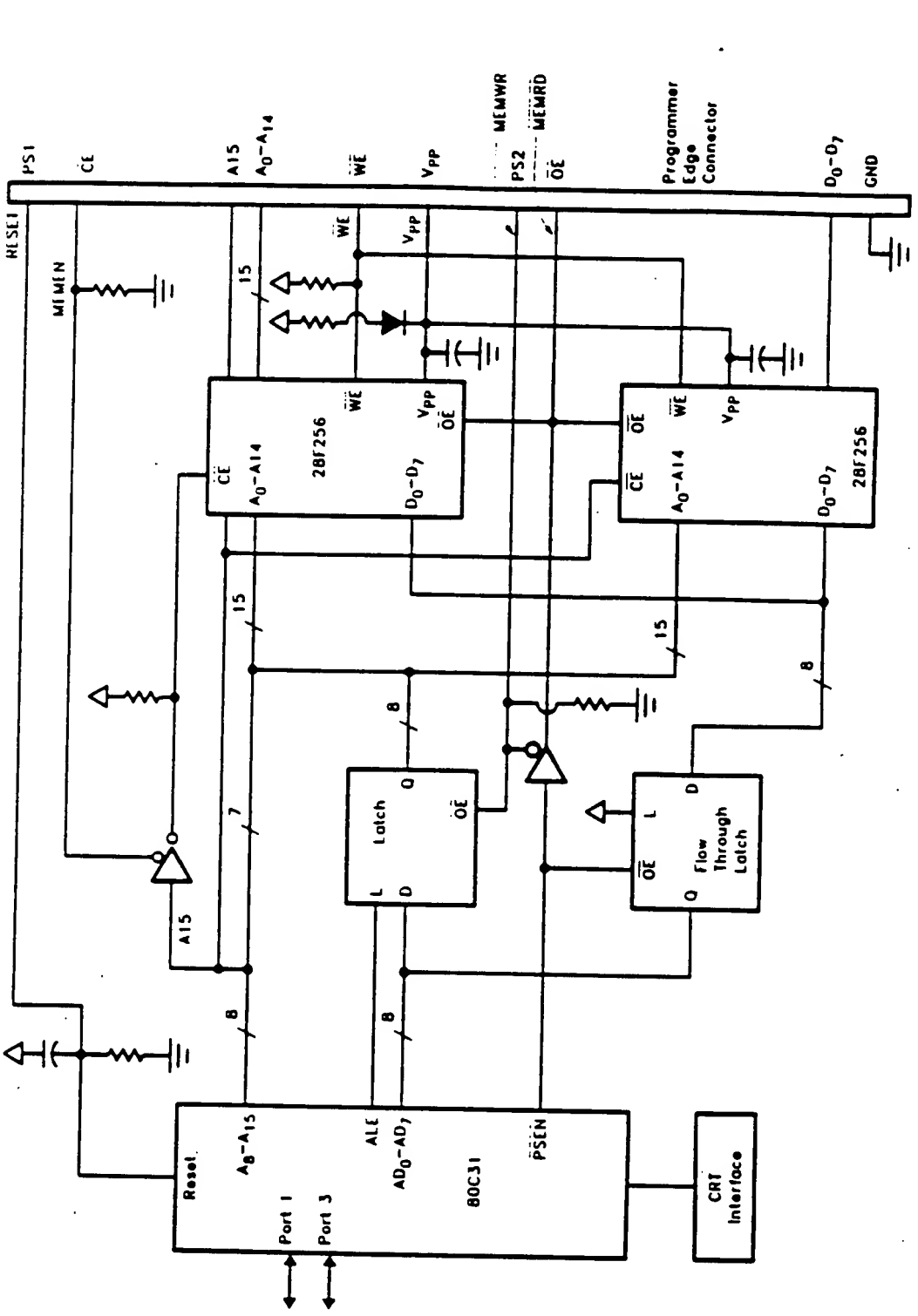


Figure 3. System Block Diagram

SAN040072

This is accomplished as illustrated. When A15 is low, the lower 32K bytes are selected. The output of the inverter drives the other 28F256's chip enable. This type of memory architecture promotes power savings by disabling all memories but the one being addressed.

To accomplish this two-line memory control architecture, route the inverters input A15 to the 80C31 and to the programmer interface connector.[8] The board-programmer controls the inverter's output enable with $\overline{MEMEN}$.[9] The $\overline{MEMEN}$ line performs the function normally performed by $\overline{CE}$ in component programming. When driven to a logic "1" level $\overline{MEMEN}$ pulls the inverter's output high. This deselects all memory devices controlled by that I.C. During normal read and standby operations, the pull-down on $\overline{MEMEN}$ keeps the decoder enabled.

Erasure and Programming Control Circuitry

In this design, V_{PP} and $\overline{WE}$ are active only during reprogramming. At other times, the two inputs would be inactive. Simply tie the $\overline{WE}$ line to V_{CC} through a pull-up resistor. The pull-up limits the current to the board programmer during reprogramming. (Recall that $\overline{WE}$ is active low.) Flash memories allow V_{PP} to be at 12V, V_{CC} or ground for read operations. This design ties V_{PP} to V_{CC} through a diode and resistor to allow for EPROM OBP compatibility. If this option is not required, simply tie V_{PP} to ground through a current-limiting pull-down resistor.

Returning Control to the Host System

The board-programmer should return system-control to the host processor in an organized manner. First it should lower V_{PP} from 12V to 5V, or ground. Then the board programmer should place its address and data buses into a high impedance state. Next PS2, which controls MEMWR should be tristated thus disabling the $\overline{PSEN}$/Address latch isolation. Finally the board-programmer should switch PS1, which drives the RESET line to reactivate the µC. This sequence guarantees that the µC will begin operation at a known program code location.

16-BIT BUS DESIGN CONSIDERATIONS

An example of an On-Board programmable 16-bit system board would be an 80C186 microprocessor, two 28F010 flash memories, RAM, and some glue chips. The basic hardware design considerations would be the same as those in the previously discussed 8-bit bus example.

There are a few issues with 16-bit designs that do not arise in 8-bit designs. For the programmer to take control of the system, it must tristate and reset the µP as well as tristate the bus buffers and latches. The HOLD and RESET lines of Intel's 86-based family of microprocessors have been designed with bus isolation in mind for use in multiprocessor systems.

The designer has two options for erasing and programming the high and low bytes of the flash memory array independently.

1) The designer can route two $\overline{WE}$ lines to the programmer connector—BYTE HIGH $\overline{WE}$ and BYTE LOW $\overline{WE}$.

2) The reprogramming software can follow the masking procedure shown in section 4.4. This method allows a common $\overline{WE}$ line for the high and low bytes.

8. Note the lack of isolation buffers between the 80C31's high order addresses (Port 2) and the board-programmer interface, compared to the latch separating the low order addresses (Port 0) and the interface. In this design example, we make use of the 80C31's ability to tristate these ports, so no isolation is needed for any of the addresses. The latch on Port 0 is for the time-multiplexed address/data architecture of this microcontroller, and not specifically for isolation.
9. MEMEN = memory enable, active low.

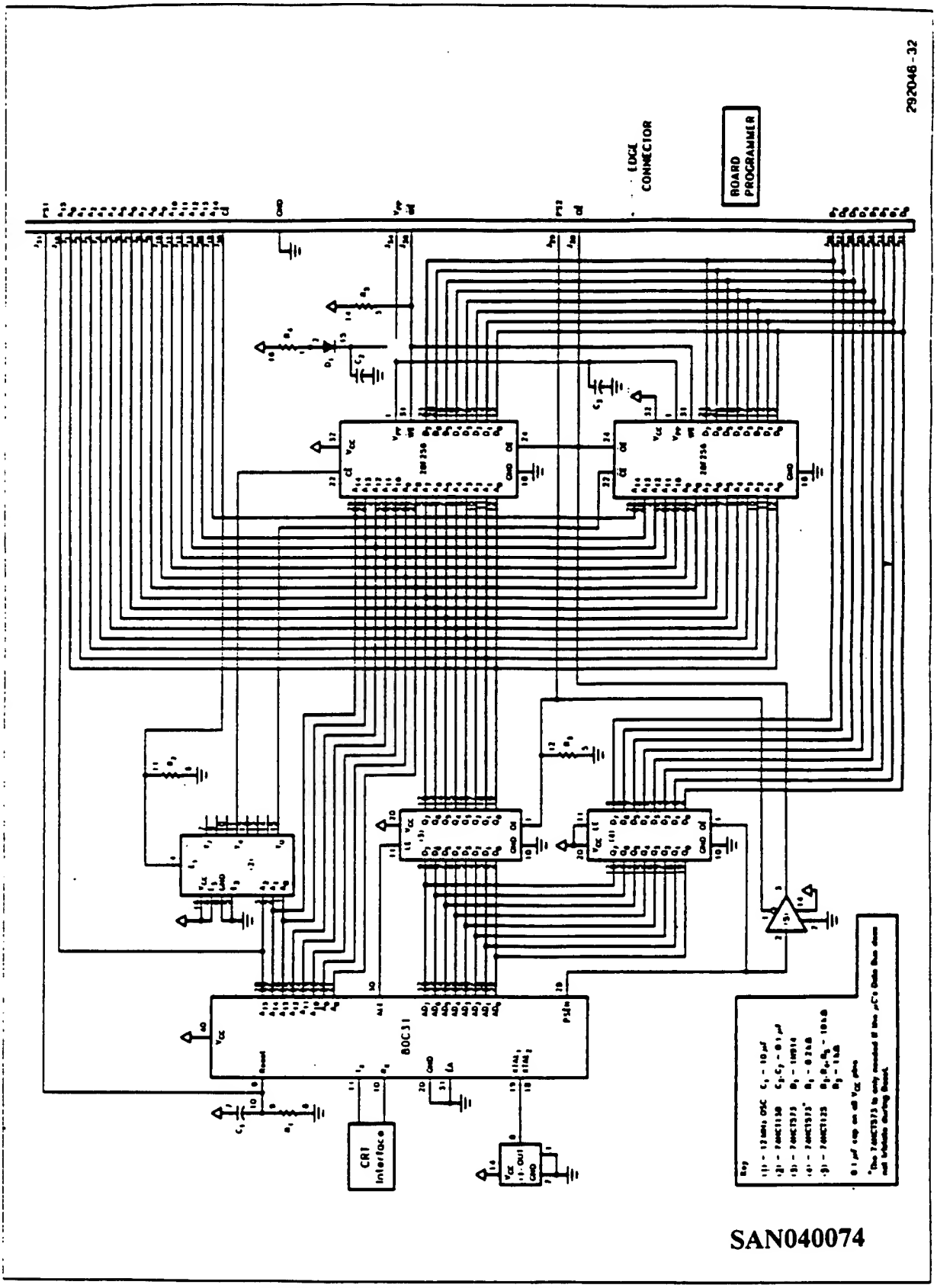


Figure 4. Detailed 8-Bit Bus Design Schematic

OBP EQUIPMENT AND VENDORS

If you are considering OBP for your next design, and have not used on-board programming before, you will need to choose a board-programmer vendor. Various suppliers offer OBP systems; therefore, it is well worth it to send out requests for programming support bids. If your production volume justifies the purchase of more than one board-programmer, you may want to negotiate a non-recurring engineering charge for development cost, followed by variable costs for additional units.

Most vendors offer a variety of basic systems, designed to easily adapt to your needs. Systems can be purchased that program either single boards serially, or a number of boards in parallel. Light-weight OBP equipment designed for field reprogramming can also be obtained from some of the vendors.

Most companies will work directly with you at the beginning of your design phase to ensure OBP compatibility. If your design is beyond the definition stage, the programmer manufacturer will request a copy of your schematics or block diagrams under non-disclosure. The vendor has an OBP design specialist that will check the design for OBP compatibility. Any potential problems will be located and corrected at this early stage.

Every board's architecture is different (i.e., based on different central processing units (CPU), decoding schemes, buffering methodologies, interface connectors, and types and densities of memories). Vendors write custom software modules for each application. Also, the vendor or the board designer typically builds an interface jig to connect the board's edge connector to the programmer. This choice is often left as a decision for the designer.

Partial List* of Companies Selling Board-Programmers

Following are a few of the companies who offer on-board programming solutions today

Data I/O Corp.
Digelec
Elan Digital Systems
Oliver Advanced Engineering, Inc.
Stag Microsystems, Inc.

*This list is intended for example only, and in no way represents all companies that support on-board programming. Intel Corporation assumes no responsibility for circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

SUMMARY

- On-board programming (OBP) has been around since 1981.
- Designing a board for OBP can be easily done by working with a board-programmer vendor's OBP-design-specialist during the initial design phase.
- In-circuit alterable code storage can be easily implemented by using flash memory and it's features.
- Time and money savings can be realized in a number of ways by taking advantage of flash memory OBP:

< > Decreased board costs and improved reliability from elimination of EPROM sockets.

< > Decreased manufacturing costs from elimination of board eraser depreciation costs, recurring U.V. light bulb and energy expenses;

< > Decreased inventory expense from simplified test and rework methods (one-step diagnostics, erasure, and board configuration);

< > Decreased product costs based on decreased board-handling loss.

< > Improved board diagnostics and testability leading to higher quality and decreased customer returns; and

< > **Quicker, more reliable field code updates.**

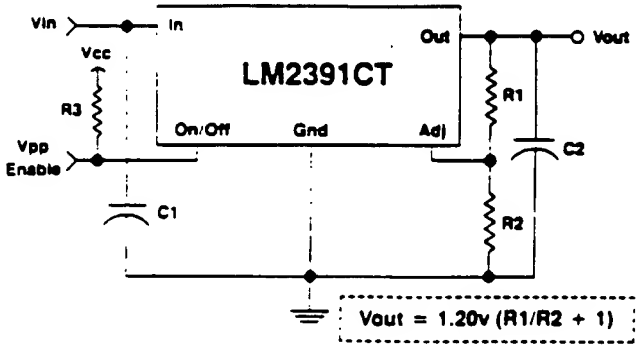
SAN040075

APPENDIX B
V_{PP} GENERATION CIRCUITS

Circuit #1—Regulation from a higher voltage
Circuit #2—Regulation from a higher voltage
Circuit #3—Regulation from a higher voltage
Circuit #4—5V to 12V Boost
Circuit #5—5V to 12V Boost
Circuit #6—Monolithic DC/DC Convertor

Circuit #1

Down Conversion
(From 14.0V–26.0V to 12.00V)



292046-12

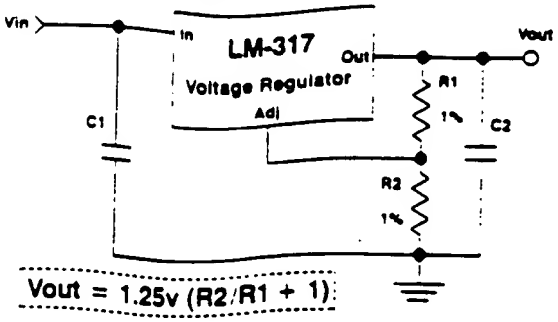
COMPONENTS	COST*
LM2391CT	$0.75
R1 = 20 KΩ, 1%	0.045
R2 = 180 KΩ, 1%	0.045
R3 = 10 KΩ	0.02
C1 = 0.1 μF	0.02
C2 = 100 μF	0.15
	$1.03

NOTES:
—The LM2391 offers an enable pin for added data protection.
—The drop out voltage is 0.6V.
—R3 is NOT required if V_{PP} enable is driven by a CMOS device.
*Cost approximations assume 10,000 piece quantity.

SAN040076

Circuit #2

Down Conversion
(From 16.00V–26.00V to 12.00V)



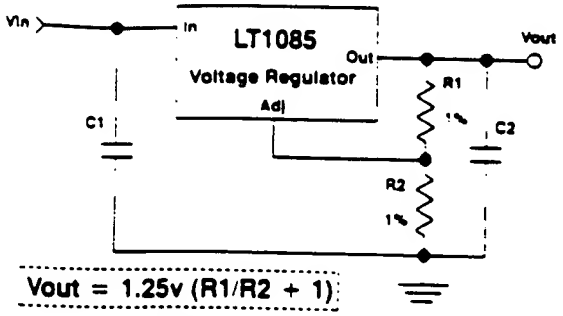
292046-13

COMPONENTS	COST*
LM-317	0.40
R1 = 124Ω, 1%	0.045
R2 = 1070Ω, 1%	0.045
C1 = 0.1 μF	0.02
C2 = 100 μF	0.15
	$0.66

NOTES:
LM-317 requires a minimum $V_{IN}-V_{OUT}$ = 3.0V
*Cost approximations assume 10,000 piece quantity.

Circuit #3

Down Conversion
(From 15.0V–40.0V to 12.00V)



292046-14

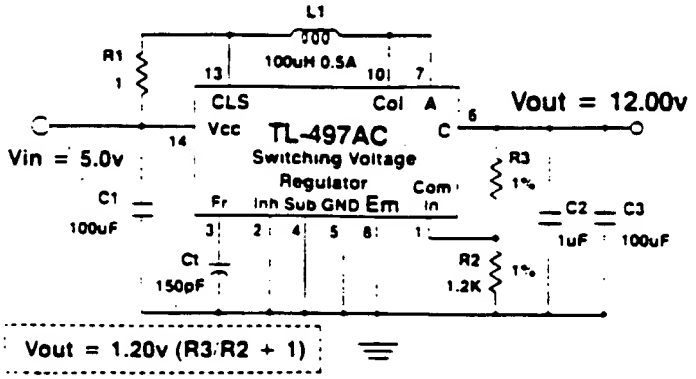
COMPONENTS	COST*
LT-1085	2.50
R1 = 124Ω, 1%	0.045
R2 = 1070Ω, 1%	0.045
C1 = 10 μF	0.10
C2 = 10 μF	0.10
	$2.79

NOTES:
LT-1085 requires a minimum $V_{IN}-V_{OUT}$ = 1.5V
*Cost approximations assume 10,000 piece quantity.

SAN040077

Circuit #4

Up Conversion Circuit
(From 5.0V to 12.0V)



292046-15

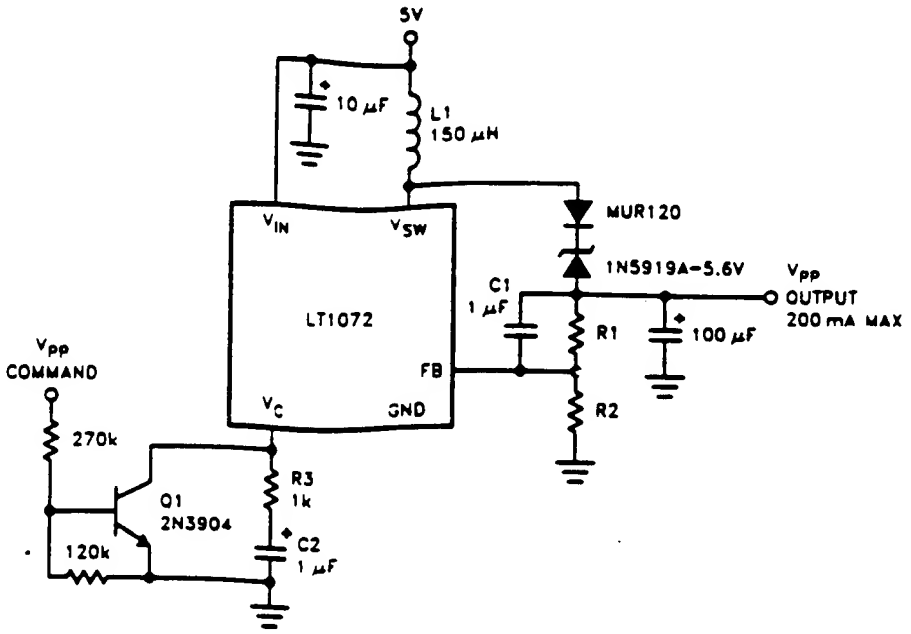
COMPONENTS	COST*
TL-497AC	1.15
R1	0.02
R2	0.045
R3	0.045
C1	0.15
C2	0.15
C3	0.02
L1	1.00
Ct	0.02
	$2.600

NOTE:
*Cost approximations assume 10,000 piece quantity.

SAN040078

Circuit #5

Up Conversion
(From 5V to 12.0V)



292046-33

COMPONENTS	COST*
LT1072	1.82
R1 = 10.7k, 1%	0.045
R2 = 1.24k, 1%	0.045
R3 = 1k, 5%	0.02
R4 = 120k, 5%	0.02
R5 = 270k, 5%	0.02
C1 = 1 µF	0.10
C2 = 1 µF	0.10
C3 = 10 µF	0.15
L1 = 150 µH	1.00
Q1 = 2N3904	0.10
	$3.42

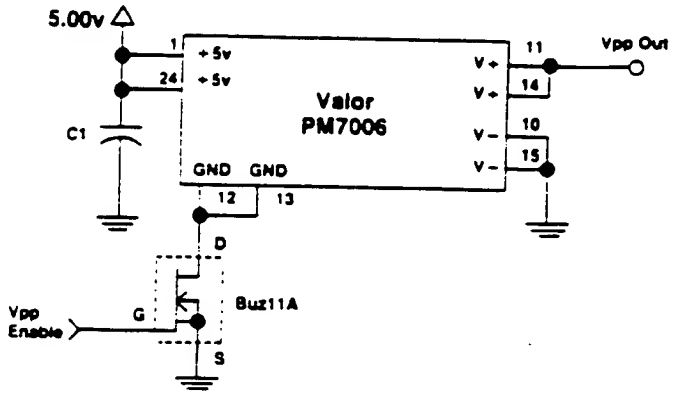
VppOUT	R1	R2	Resistor Tolerance
12.0V	10.7k	1.24k	1%

NOTES:
Drive VPP COMMAND low to turn on the circuit.
*Cost approximations assume 10,000 piece quantity.

SAN040079

Circuit #6

Up Conversion Circuit
(From 5.0V to 12.0V)



292046-16

COMPONENTS	COST*
PM7006	$6.25
C1 = 0.1 μF	0.05
Buz11A	2.59
	$8.89

NOTES:
1. The capacitor decreases output noise to 140 mV pk-pk.
2. We added the Buz11A Mospower nFET to enable/disable the converter. This control minimizes power consumption which under full load can reach 600 mA.
3. The voltage drop across the switch is 0.1V. Due to this drop the PM7006 will not maintain the V_{PP} spec with 10% fluctuations in V_{CC} supply.

*Cost approximations assume 10,000 piece quantity.

SAN040080

APPENDIX C
LIST OF DC-DC CONVERTER COMPANIES

BURR-BROWN
P.O. Box 11400
Tucson, AZ 85734
(602) 746-1111

CARITRONICS INC.
P.O. Box 821
West Caldwell, NJ 07007
(201) 575-8916

LINEAR TECHNOLOGY CORP.
1630 McCarthy Blvd.
Milpitas, CA 95035-7487
(408) 432-1900

NOVA-TRONIX
4701 Patrick Henry Dr. #24
Santa Clara, CA 95054
(408) 727-9530

RELIABILITY INC.
(713) 492-0550

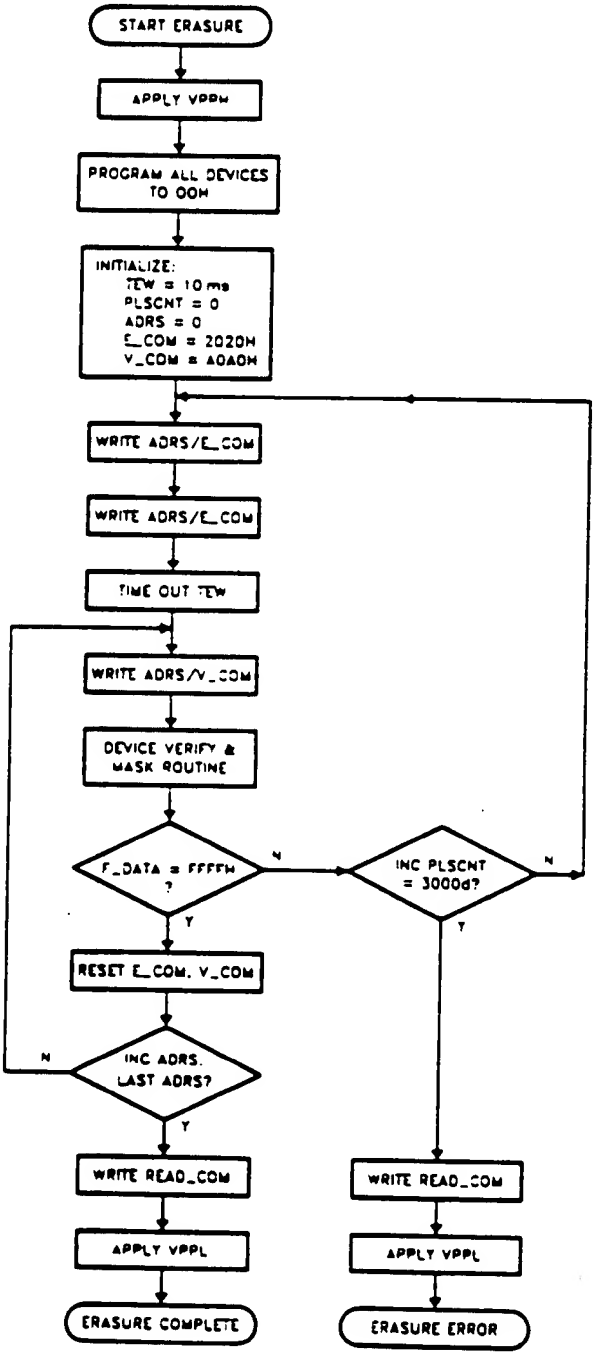
SEMICONDUCTOR CIRCUITS INC.
49 Range Road
Windham, New Hampshire 03087
(603) 893-2330

UNIVERSAL MICROELECTRONICS
Marcon Sales Inc.
2672 Bayshore Parkway, Suite 1000
Mountain View, CA 94043
(415) 964-8040

VALOR ELECTRONICS
9275 Nancy Ridge Dr.
San Diego, CA 92121
(619) 458-1471

SAN040081

APPENDIX D
PARALLEL ERASE FLOW CHART

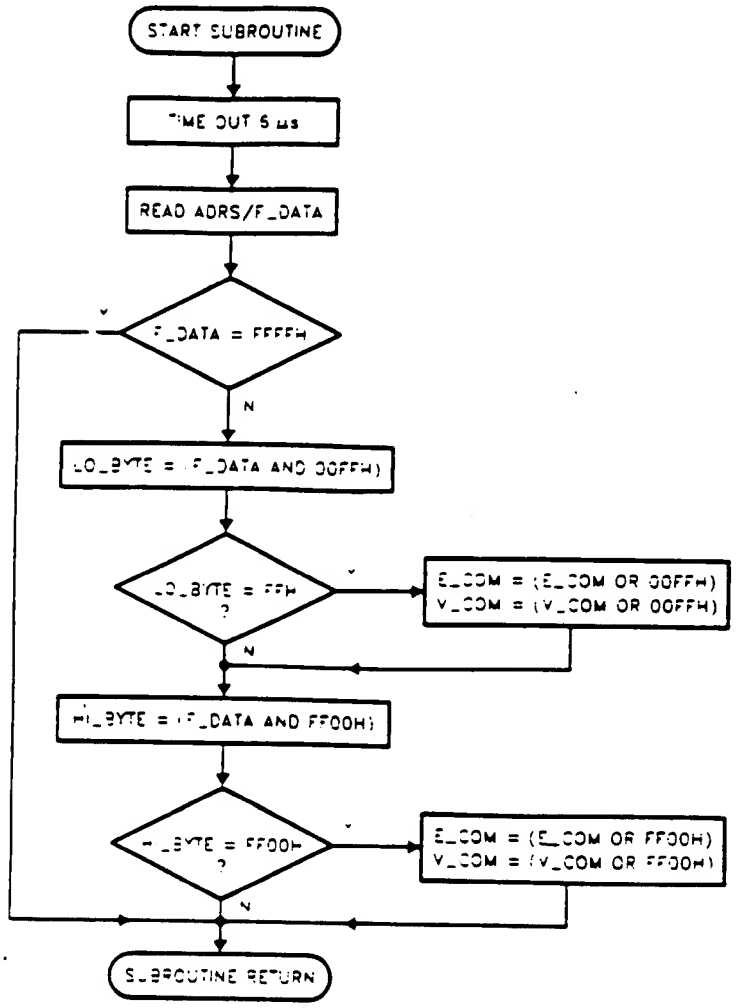


292046-34

COMMENTS
Wait for V_{PP} to stabilize.
Use Quick-Pulse Programming algorithm.
Initialize Variables: TEW = Erase duration (width) PLSCNT = Pulse Counter ADRS = Address E_COM = Erase Command V_COM = Verify Command
Erase Set-up Command
Start Erasing
Duration of Erase Operation.
Erase Verify Command stops erasure.
See next page for subroutine.
When both devices at ADRS are erased, F_DATA = FFFFH. If not equal, increment the pulse counter and check for last pulse.
Reset commands to default (E_COM = 2020H, V_COM = A0A0H) before verifying next ADRS.
Reset devices for read operation.
Turn off V_{PP}.

SAN040082

Device Verify and Mask Subroutine



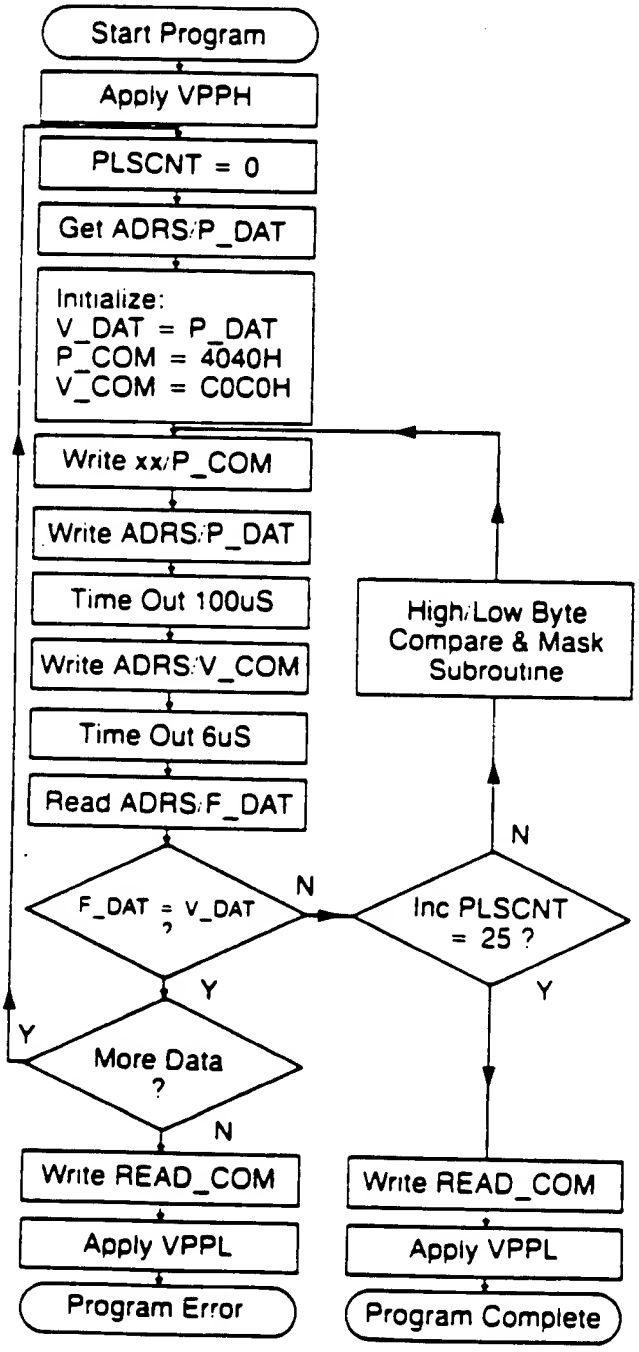
COMMENTS
This subroutine reads the data word (F__DATA). It then masks the HI or LO Byte of the Erase and Verify commands from executing during the next operation.
If both HI and LO bytes verify, then return.
Mask* the HI Byte with 00H
If the LO Byte verifies erasure then mask* the erase and verify commands with FFH(Reset).
Mask* the LO Byte with 00H.
If the HI Byte verifies erasure, then mask* the erase and verify commands w/FF00H(Reset).

232046-35

NOTE:
*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming flash data (F__DATA), the erase commands and the verify commands. Then manipulate the HI or LO register contents.

SAN040083

APPENDIX E
PARALLEL PROGRAMMING FLOW CHART

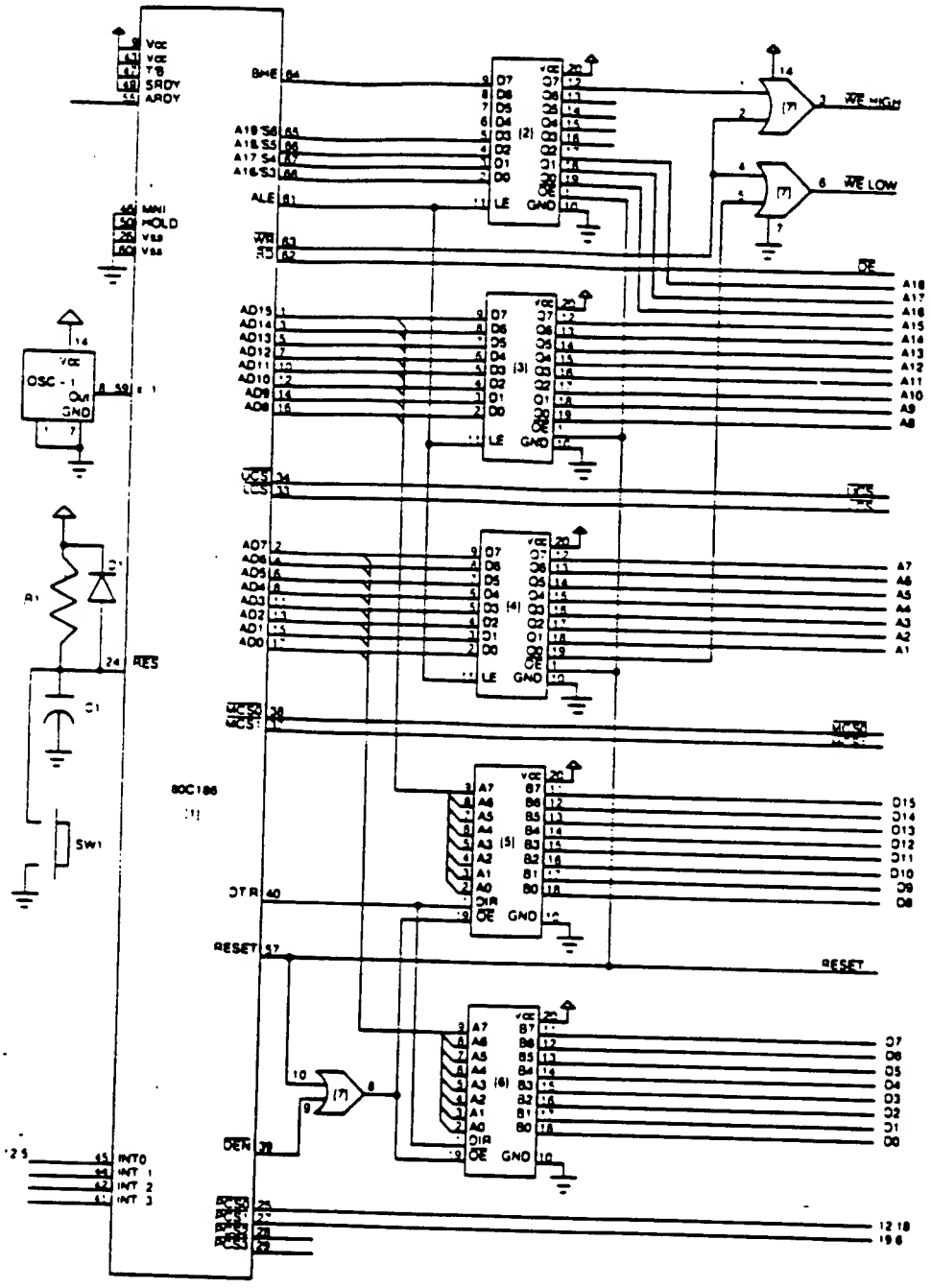


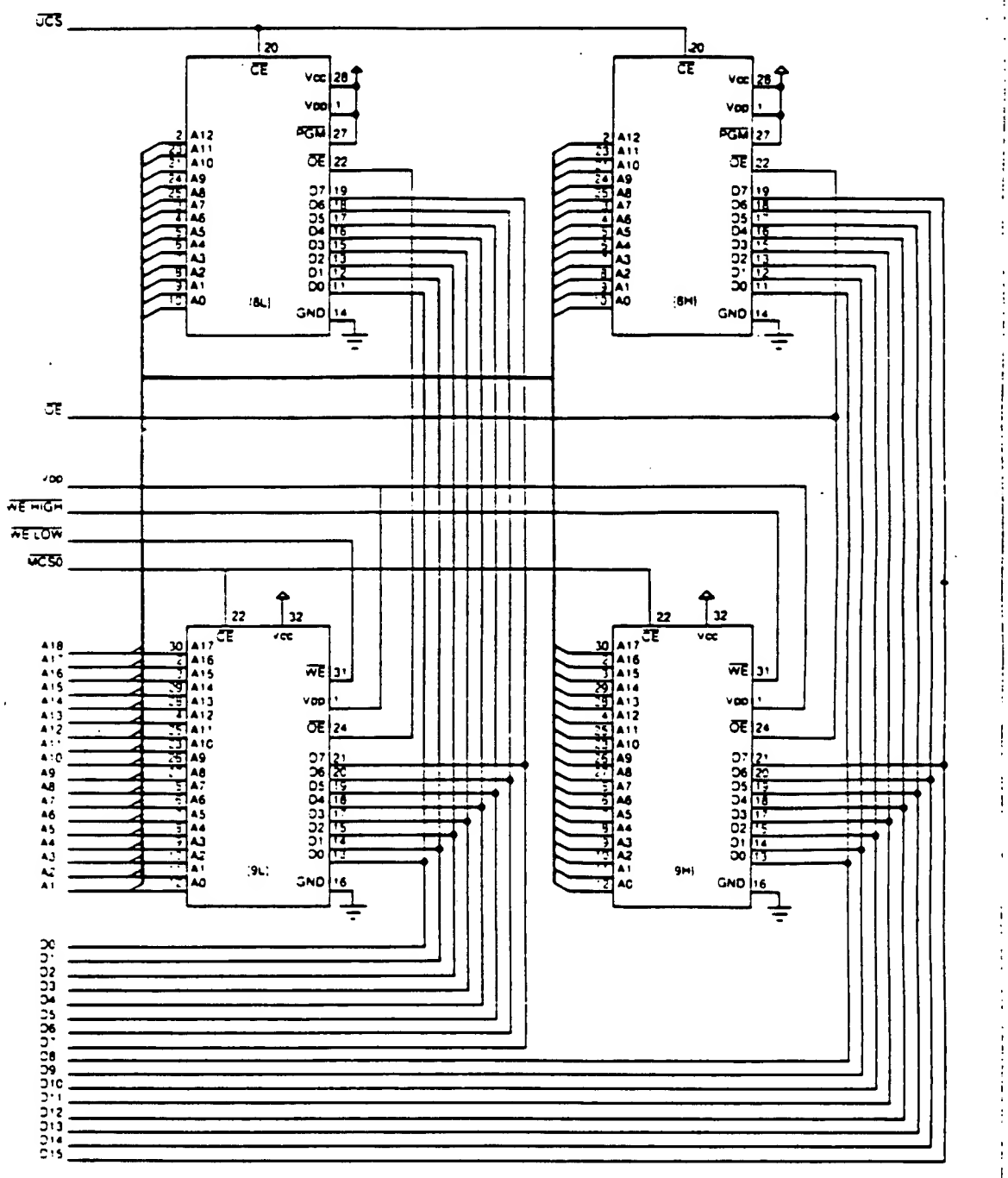
COMMENTS
Wait for V_{CC} ramp to V_{PPH}
PLSCNT = Pulse Counter
ADRS = address to program P_DAT = data word to program
Initialize Data Word Variables: V_DAT = valid data P_COM = Program Command V_COM = Verify Command
Program Set-up Command xx = Address don't care
Program
See next page for subroutine
Program Verify Command
F_DAT = flash memory data
Compare flash memory data to valid data (word compare). If not equal, increment pulse counter & check for last pulse. If not last pulse, compare High and Low Byte.
Check buffer or I/O port for more data to program.
Reset device for read operation.
Turn off V_{PP}.

292046-19

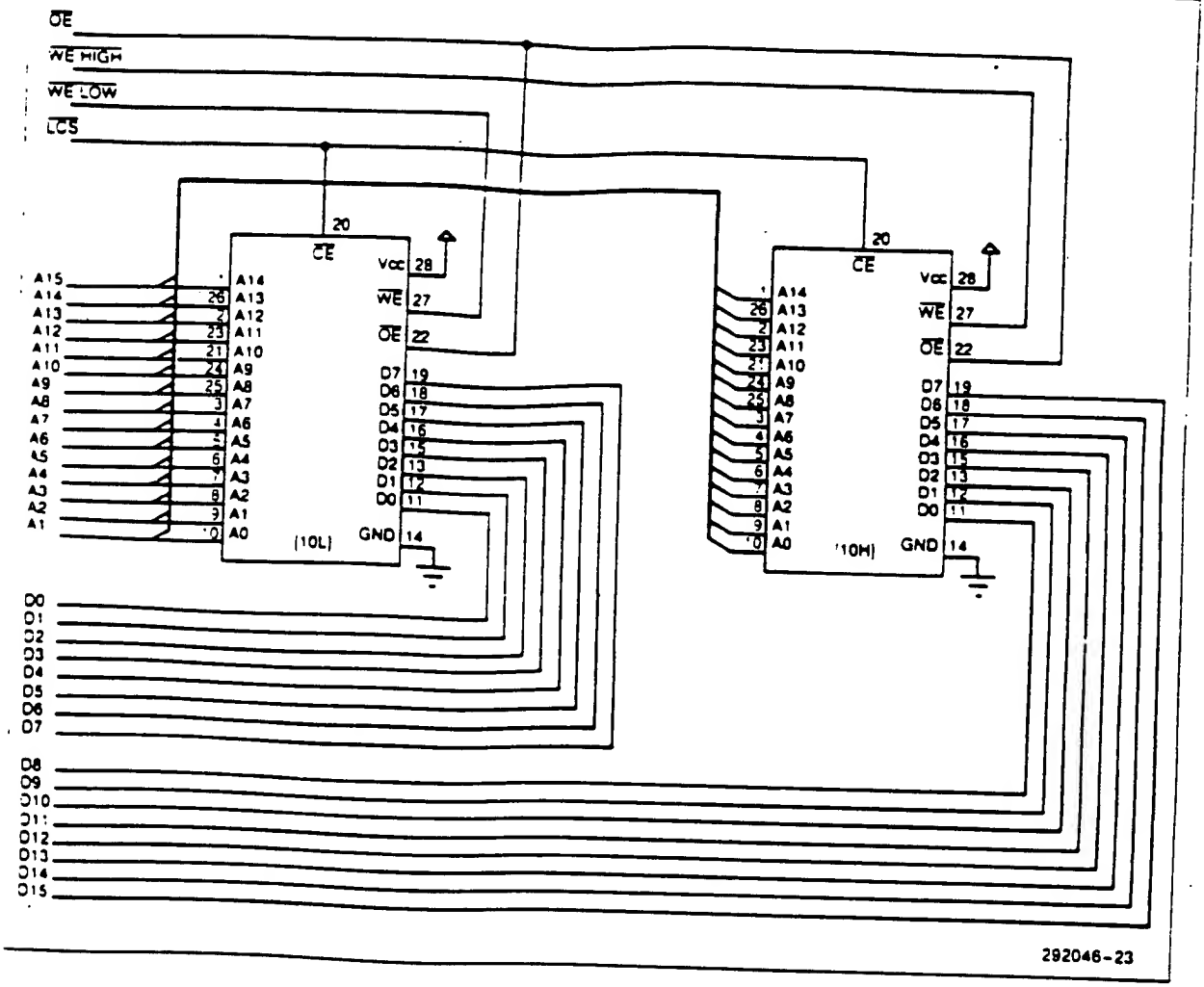
SAN040084

APPENDIX F
DETAILED SYSTEM SCHEMATICS




UCS
OE
VDD
WE HIGH
WE LOW
MCS0
CE
VCC
VPP
PGM
OE
WE
GND
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
(8L)
(8H)
(9L)
(9H)
292046-22

SAN040086


OE
WE HIGH
WE LOW
LCS
20
CE
Vcc 28
WE 27
OE 22
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7 19
D6 18
D5 17
D4 16
D3 15
D2 13
D1 12
D0 11
GND 14
(10L)
(10H)
D0
D1
D2
D3
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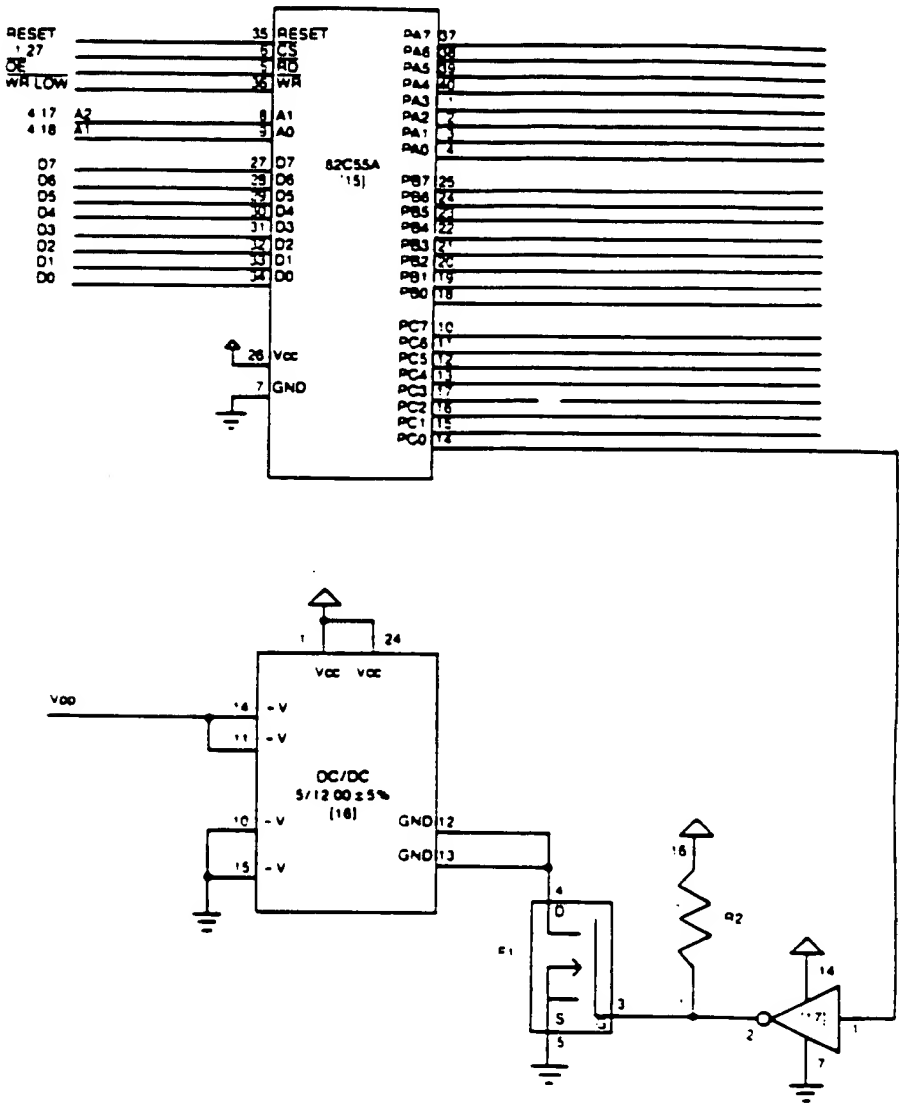
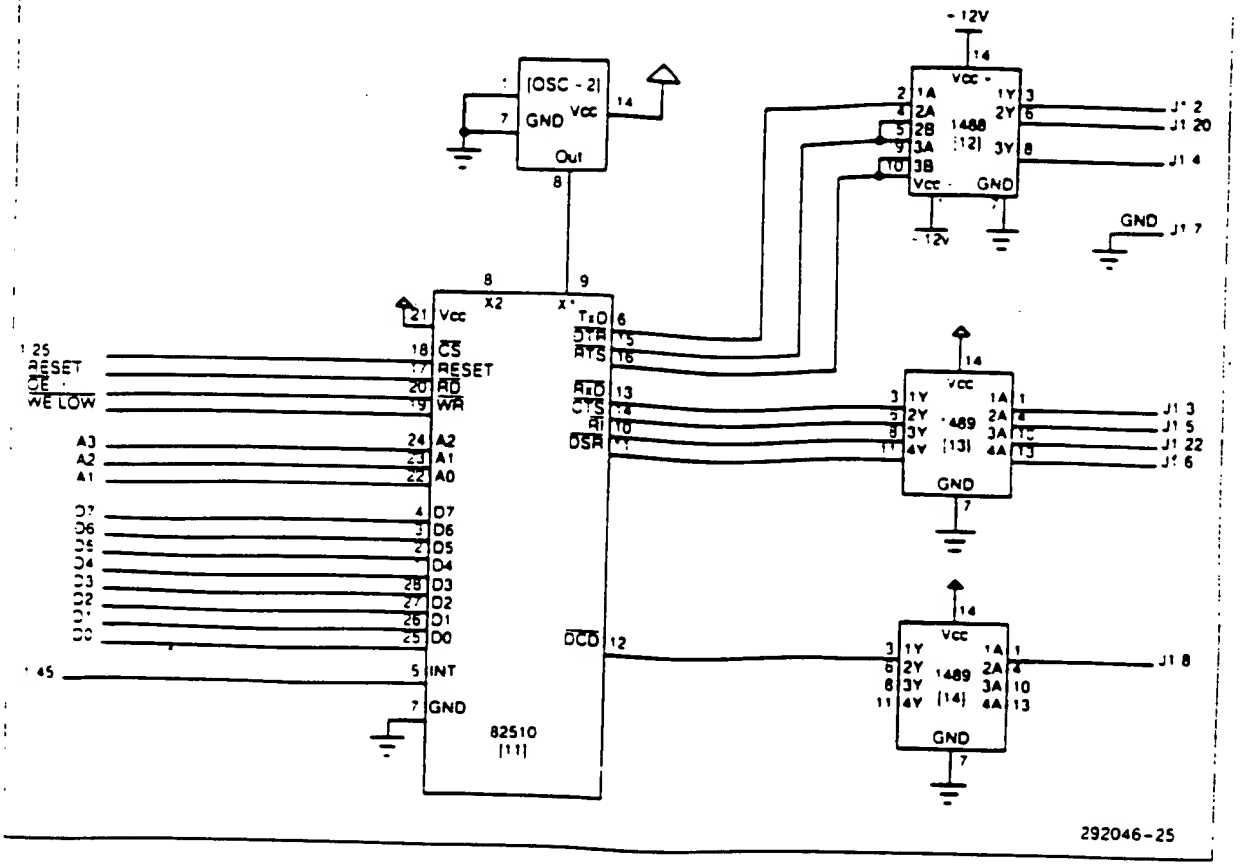
D12
D13
D14
D15
292046-23

SAN040087



292046-24

SAN040088


-12V
(OSC - 2)
GND
Vcc
Out
82510
(11)
X2
Vcc
CS
RESET
RD
WR
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
INT
GND
TxD
RTS
RxD
CTS
RI
OSR
DCD
1488
(12)
1A
2A
2B
3A
3B
1Y
2Y
3Y
4Y
GND
J1 2
J1 20
J1 4
J1 7
1489
(13)
J1 3
J1 5
J1 22
J1 6
1489
(14)
J1 8
WE LOW
292046-25

256K FLASH MEMORY DEMO PARTS LIST

Device	Component	Pins	Description
[1]	80C186	68	16-bit high integration CPU
[2,3,4]	74HC573	20	Latch
[5,6]	74HC245	20	Transceiver
[7]	74HC32	14	OR gate
[8L,8H]	27C64	28	16 Kbyte EPROM
[9L,9H]	28F256	32	64 Kbyte flash memory
[10L,10H]	32K x 8 SRAM	28	64 Kbyte SRAM
[11]	82510	28	Asynchronous Serial Controller
[12]	14C88	14	RS-232 Line Driver
[13,14]	14C89	14	RS-232 Line Receiver
[15]	82C55A	40	Programmable Peripheral Controller
[16]	PM7006	24	DC/DC Convertor (5V–12.00V)
[17]	7406	14	Invertor—Open Collector (O.C.)
C1	20 μF	2	Capacitor for CPU reset
D1	1N914	2	Diode for CPU reset
F1	BUZ11A	3	MOSPOWER nFET
J1	DB-25	25	Connector (male)
OSC-1	20 MHz	14	CPU Oscillator
OSC-2	18.432 MHz	14	Serial Controller Oscillator
R1	10 KΩ	2	¼W, 10% Resistor for CPU reset
R2	1 KΩ	2	¼W, 10% Resistor for O.C. pull-up
SW1		3	Momentary Push Button for CPU reset

NOTES:
1. Place a 0.1 μF bypass capacitor at the V_{CC} input of each IC.
2. Place a 0.1 μF bypass capacitor on the V_{PP} input of each 28F256 flash memory.

28F512 UPGRADE FOR THE 80C186/FLASH MEMORY DESIGN

To upgrade the 80C186/Flash memory design to handle 28F512's, the range of the $\overline{CE}$ signal has to be increased. There are a number of ways to generate a $\overline{CE}$ signal that will span the 128 Kbyte address range of two 28F512 devices.

1. AND two of the current MCS lines together (defined for 64 Kbytes each); or
2. Change the MCS individual block-select size from 64 Kbytes:

   MMCS_VALUE = 41F8H,
   MPCS_VALUE = 0A0B8H

   to 128 Kbytes:

   MMCS_VALUE = 01FEH,
   MPCS_VALUE = 0C0BEH

   Also, cut the $\overline{CE}$ trace to the RAM sockets. Then wire $\overline{MCS0}$ to the RAM $\overline{CE}$. This eliminates the $\overline{MCS0}$ and $\overline{LMCS}$ range overlap caused by increasing the MCS range to 128 Kbytes. See 80C186 Data Sheet page 21 and 22 (Order # 270354).

SAN040090

28F010 UPGRADE TO THE 80C186/FLASH MEMORY DESIGN

To upgrade the 80C186/Flash memory design to handle 28F010's, a $\overline{CE}$ signal has to be generated. There are a number of ways to generate a $\overline{CE}$ signal that will span the 256 Kbyte address range of two 28F010 devices.

1. **AND two of the MCS lines together** (defined for 128 Kbytes each as noted in the 28F512 modifications):

   Cut the LMCS trace to the RAM sockets. Connect $\overline{MCS0}$ to $\overline{CE}$ on the RAM sockets (U10L,UH).

   Cut the $\overline{MCS2}$ trace to the flash memory. Add an AND gate. Connect $\overline{MCS2}$ (cut trace) and $\overline{MCS3}$ to the inputs of the AND gate. Then wire the AND gate output to the $\overline{CE}$ of the flash memories.

   Also, change the onboard memory MCS register to:
   MMCS_VALUE = 01FEH, MPCS_
   VALUE = 0C0BEH [128K blocks],

   and delete:
   LMCS_REG and LMCS_Value.

2. **Add a decoder:**

   Add a decoder (74HC138). Connect address lines A18 and A19 to the B and C inputs of the decoder. Tie the A input of the decoder low, and enable all the enables. By using outputs Y0, Y2, Y4, and Y6, you have four $\overline{CE}$ lines decoding 256 Kbyte blocks each.

   Cut the $\overline{MCS2}$ trace to the flash memories. Connect the Y2 output from the decoder to the $\overline{CE}$ input of the flash memory.

3. **Replace the address latch (U2) with a PLD that latches and decodes.**

   Program a 5C032 as an integrated latch and decoder. Replace the upper address latch [U2] with the Intel 5C032 EPLD. Cut the $\overline{CE}$ trace to the flash memories. Connect the flash memories' $\overline{CE}$ to the 5C032 pin 12. This maps the address space 40000H to 7FFFFH. See Figures 1 and 2 for a comparison of the 74HC573 (U2) and programmed 5C032 pin outs. Figure 3 is the source code for the EPLD.

   Also, change the value of the MMCS and MPCS registers to 64 Kbyte blocks so that the $\overline{MCS0}$ range does not overlap the LMCS range.
   MMCS_VALUE = 41F8H, MPCS_
   VALUE = 0A0B8H.

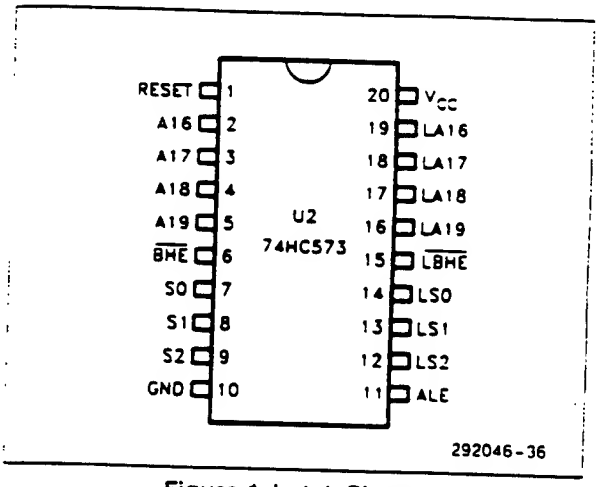


Figure 1. Latch Pinout

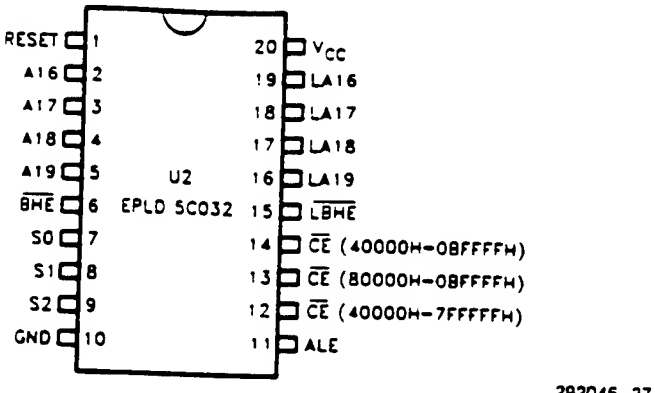


Figure 2. Integrated Latch and Decoder

SAN040091

```
Thom Bowns - PLFG Applications
Intel
January 13, 1989
EPLD HOTLINE: 1-800-323-EPLD
002
5C032
Custom Latched Decoder
OPTIONS: TURBO=ON
PART: 5C032

INPUTS: ALE@11, RESET@1, A19@5, A18@4, A17@3, A16@2, nBHE@6

OUTPUTS:  LA18@17, LA17@18, LA16@19, LnBHE@15, nCE3@14, LA19@16,
          nCE2@13, nCE1@12

NETWORK:
          ALE = IN (ALE)
          RESET = INP (RESET)
          nRESET = NOT (RESET)
          A19 = INP (A19)
          A18 = INP (A18)
          A17 = INP (A17)
          A16 = INP (A16)
          nBHE = INP (nBHE)
          LA19, LA19 = COIF (LA19d, nRESET)
          LA18, LA18 = COIF (LA18d, nRESET)
          LA17, LA17 = COIF (LA17d, nRESET)
          LA16, LA16 = COIF (LA16d, nRESET)
          LnBHE, LnBHE = COIF (LnBHE, nRESET)
          nCE3, nCE3 = COIF (nCE3, nRESET)
          nCE2, nCE2 = COIF (nCE2, nRESET)
          nCE1, nCE1 = COIF (nCE1, nRESET)

EQUATIONS:
          LA19d = A19 * ALE + LA19 * !ALE;
          LA18d = A18 * ALE + LA18 * !ALE;
          LA17d = A17 * ALE + LA17 * !ALE;
          LA16d = A16 * ALE + LA16 * !ALE;
          LnBHEd = nBHE * ALE + LnBHE * !ALE;
          nCE3d = nCE3EQN * ALE + nCE3 * !ALE;
          nCE2d = nCE2EQN * ALE + nCE2 * !ALE;
          nCE1d = nCE1EQN * ALE + nCE1 * !ALE;
          nCE2EQN = !(A19 * !A18);
          nCE1EQN = !(!A19 * A18);
          nCE3EQN = !(!A19 * A18 + A19 * !A18);

END$
```

Figure 3. Source Code for the Integrated Latch and Decoder

SAN040092

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ENGINEERING REPORT

ER-20

September 1989

ETOX™II Flash Memory Technology

JASON ZILLER
PRODUCT ENGINEERING

SAN040093

Order Number: 294005-006

INTRODUCTION

Intel's ETOX™ II (EPROM tunnel oxide) flash memory technology is derived from the CHMOS** III-E EPROM technology. It replaces ultraviolet erasability with a non-volatile memory cell that is electrically erasable in bulk array form. Intel flash memory combines the EPROM programming mechanism with EEPROM erase, producing a versatile memory device that is highly reliable and cost effective. This report describes the fundamentals of the ETOX II flash memory cell in comparison to the standard EPROM, and gives insight into its operation in a system environment.

The ETOX II flash memory cell is nearly identical in size to CHMOS III-E EPROM. This allows comparable densities. The primary difference between ETOX II flash memory and EPROM cells is the flash memory cell's thinner gate oxide, which permits the electrical erase capability. (See Photo 1.)

ETOX™ II FLASH MEMORY CELL

Intel's ETOX II flash memory cell is composed of a single transistor with a floating gate for charge storage, like the traditional EPROM. (See Figure 1.) In contrast, conventional two-transistor EEPROM cells are typically much larger. Intel produces ETOX II flash memory devices on 1.0μ photolithography.

The ETOX II cell's programming mechanism is identical to the EPROM: that is, hot channel electron injection. The device programming mode forces the cell's control gate and drain to a high voltage while leaving the source grounded. The high drain voltage generates "hot" electrons that are swept across the channel. These hot electrons collide with other atoms along the way, creating even more free electrons. Meanwhile, the high voltage on the control gate attracts these free electrons across the lower gate oxide into the floating gate, where they are trapped. (See Figure 2.) Typically, this process takes less than 10 μs.

Flash memory's advantage over EPROM is electrical erasure, discharging the floating gate without ultraviolet light exposure. The erase mechanism is an EEPROM adaptation which uses "Fowler-Nordheim"[1] tunneling. A high electric field across the lower gate oxide pulls electrons off the floating gate. The erase mode routes the same external voltage used for programming to the source of the memory cell, while the gate is grounded and the drain is left disconnected. (Figure 3.)

MEMORY ARRAY CONSIDERATIONS

The ETOX II flash memory cells have the same array configuration as standard EPROM, thereby matching EPROM in density. Also, identical peripheral circuitry for normal access achieves the same read performance as the Intel CHMOS III-E EPROMs.

Intel flash memory's programming circuitry is also identical to Intel's EPROM designs. Row decoders drive the selected wordline to high voltage, while input data combined with column decoders determine the number of bitlines that are gated to high voltage. This provides the same byte programmability as an EPROM. Intel flash memories offer the efficient Quick-Pulse Programming™ algorithm that is featured on advanced EPROMs.

Array erase is unique to flash memory technology. Unlike conventional EEPROMs, which use a select transistor for individual byte erase control, flash memories achieve much higher density with single transistor cells. Therefore, the erase mode supplies high voltage to the sources of every cell simultaneously, performing a full array erasure. A programming operation must be performed before every erase to equalize the amount of charge on each cell. Then Intel's Quick-Erase™* algorithm intelligently erases the array down to the appropriate minimum threshold level required to read all "ones" data. This procedure ensures a tight distribution of erased cell thresholds throughout the array.

ETOX™ II FLASH MEMORY RELIABILITY

The reliability of Intel's CHMOS ETOX II flash memory process is equivalent to its sister EPROM technology. The ETOX II and EPROM processes share the same data retention characteristics. Preliminary qualification data shows that 1 Megabit flash memories produced on the ETOX II process provide at least 10,000 program and erase cycles with no cycling failures due to oxide stress or breakdown. In fact, several 1 Megabit flash memories were cycled past 100,000 cycles with no apparent oxide damage. This extended cycling capability is attributed to improvements in tunnel oxide processing and advantages inherent in the ETOX II cell approach.

[1] M. Lenzlinger, E.H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO2," Journal of Applied Physics, Vol. 40 (1969), p. 278.

*Intel's ETOX II flash memory process has patents pending.

**CHMOS is a patented process of Intel Corporation.

SAN040094

SUMMARY

ETOX II flash memory technology is the optimal combination of EPROM and E²PROM technologies. Intel's new ETOX II flash memory process offers extended cycling capability with the density and manufacturability of EPROMs. From an application standpoint, flash memory technology provides the capability to improve overall system quality throughout the product development and manufacturing stages. Also, flash memory density is ideally suited for applications requiring version updates of entire programs which, in turn, suit the "flash" characteristics of erasing the entire array at once. In addition, individual byte programming allows for data acquisition. Flash memory devices produce on the ETOX II process provide a high density, low cost solution to many system memory storage requirements which were previously unavailable.

Table I

	EPROM	ETOX™II Flash Memory	EEPROM
Normalized Cell Size	1.0	1.2–1.3	3.0
Programming:			
Mechanism	Hot Electron Injection	Hot Electron Injection	Tunneling
Resolution	Byte	Byte	Byte
Typ. Time	< 100 µs	< 10 µs	5 ms
Erase:			
Mechanism	UV Light	Tunneling	Tunneling
Resolution	Bulk Array	Bulk Array	Byte
Typ. Time	20 Min.	< 1 Sec.	5 ms

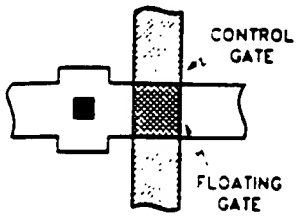

Figure 1. ETOX™II Flash Memory Cell Layout (Top View)

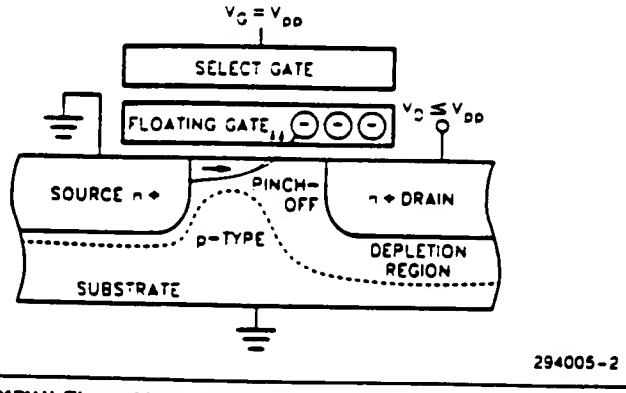

Figure 2. ETOX™II Flash Memory Cell during Programming (Side View)

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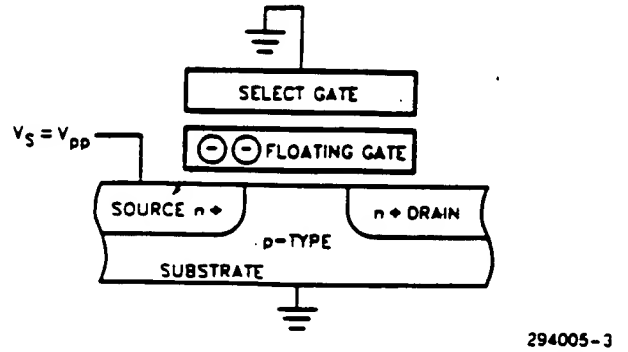
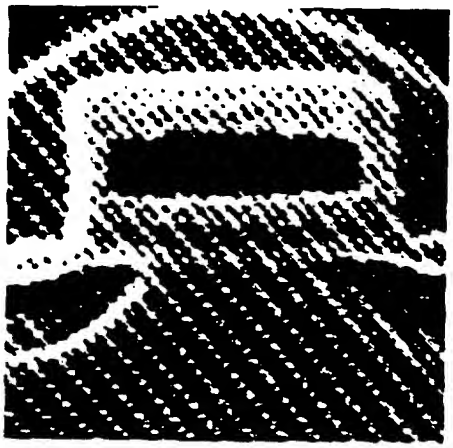


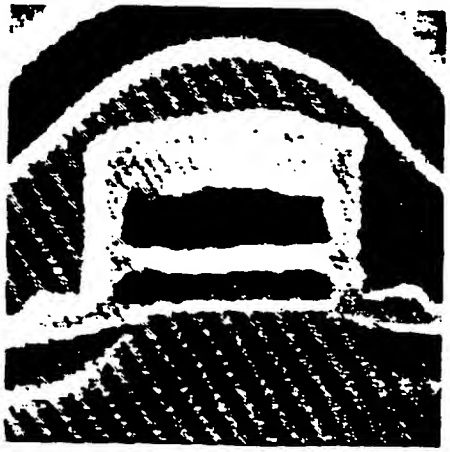
Figure 3. ETOX™II Flash Memory Cell during Erase (Side View)

PHOTO 1



294005-4

ETOX™II Cell
(50,000 x Magnification)



294005-5

CHMOS III-E EPROM Cell
(50,000 x Magnification)

SAN040096

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ENGINEERING REPORT

ER-21

September 1989

The Intel 28F256 Flash Memory

SAN040097

Order Number: 294004-003

INTRODUCTION

Intel's ETOX™ (EPROM tunnel oxide) flash memories add complete electrical chip-erasure and reprogramming to EPROM non-volatility and ease of use. Advances in tunnel oxides have made it possible to develop double-polysilicon single-transistor electrically-erasable programmable memories. Intel's ETOX flash memories electrically erase all bits in the array matrix via electron tunneling. The EPROM programming mechanism of hot electron injection is employed for electrical byte programming.

A command port interface, internal margin voltage generation, and address and data latches augment standard EPROM circuitry to make Intel's 28F256 the first high-density CMOS flash memory optimized for microprocessor-controlled reprogramming. Read timing parameters are equivalent to those of like-density CMOS EPROMs. The dense one-transistor cell structure, coupled with high array efficiency, yield a 256-kilobit die measuring 181 by 203 mils.

TECHNOLOGY OVERVIEW

ETOX flash memory technology is derived from Intel's standard CMOS EPROM process base. Using advanced CMOS 1.5um technology, the 32,768 × 8 bit flash memories employ a 6um × 6um single transistor cell, affording equivalent array density as comparable EPROM technology. The flash memory cell structure is identical to the EPROM structure except for the thinner gate (tunnel) oxide.

High quality tunnel oxide under the single floating polysilicon gate promotes electrical erasure. All cells in the array are simultaneously erased via Fowler-Nordheim tunneling. Applying 12 volts on the source junctions and grounding the select gates erases the entire array in 200ms (typical). Programming is accomplished with the standard EPROM mechanism of hot electron injection from the cell drain junction to the floating gate. Programming is initiated by bringing both the select gate and the cell drain to high voltage. Programming occurs at a rate of 100us per byte.

DEVICE ARCHITECTURE

Figure 2 illustrates the block diagram for the 28F256. Figure 4 contains the die photograph with functional blocks identified. The feature which differentiates Intel's 256-kilobit flash memory is the command port architecture.

The command port simplifies microprocessor control of the erase, erase verify, program, program verify, and read operations, without the need for additional

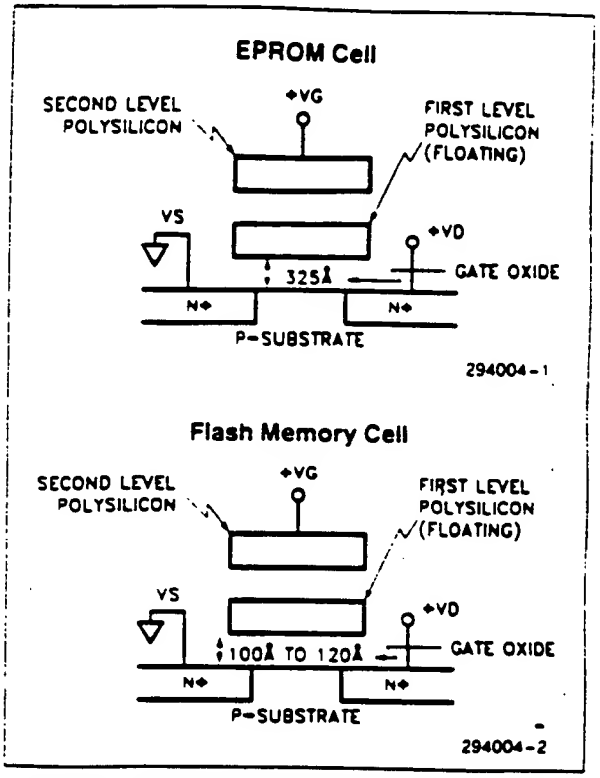

Figure 1. EPROM Cell vs. Flash Memory Cell

control pins or the multiplexing of high voltage with control functions. On-chip address and data latches minimize system interface logic and free the system bus during erase and program operations. High voltage (12V) on the Vpp pin enables the command port. In the absence of this high voltage, the device only performs the read operation, inhibiting erasure or programming of the device.

The command port consists of a command register, command decoder and state latch, the data-in latch, and the address latch. The command decoder output directs the operation of the erase voltage switch, program voltage switch, and the erase/program verify voltage generator.

Functions are selected via the command port in a microprocessor write cycle controlled by the Chip-Enable and Write-Enable pins. Contents of the address latch are updated on the falling edge of Write-Enable. The rising edge of Write-Enable latches the command and data registers, and initiates operations.

Erase is achieved through a two-step write sequence. The erase set-up code is written to the command register in the first cycle. The erase confirmation code is written in the second cycle. The rising edge of this second Write-Enable pulse initiates the erase opera-

tion. The command decoder triggers the erase voltage switch, connecting the 12V supply to the source of all bits in the array, while all wordlines are grounded. Fowler-Nordheim tunneling results in the simultaneous erasure of all bits.

Writing the erase verify code into the command register terminates erasure, latches the address of the byte to verify, and sets the internally-generated erase margin voltage. The microprocessor then accesses the output from the addressed byte using standard read timings. The verify procedure repeats for all addresses. Should a byte require more time to reach the erased state, another erase operation is applied. The erase and verify operations continue until the entire array is erased.

Programming follows a similar flow. The program set-up command is written to the command register on the first cycle. The second cycle loads the address and data latches. The rising edge of the second Write-Enable pulse initiates programming by applying high voltage to the gates and drains of the bits to be programmed.

Writing the program verify command to the register terminates the programming operation and applies the program verify voltage to the newly programmed byte. Again, the addressed byte can be read using standard microprocessor read timings. Should the addressed byte require more time to reach the programmed state, the programming operation and verification are repeated until the byte is programmed.

Erase and program verification ensure the data retention of the newly altered memory bits. The cell margining performed in the Quick-Pulse Programming™ and Quick-Erase™ algorithms is more reliable than historical overpulsing schemes as margining tests the amount of charge stored on the floating gate.

Intel's flash memories employ a unique circuit to internally generate the erase and program verify voltages. Figure 3 shows a simplified version of the circuit. The circuit consists of a high voltage switch and the verify voltage generator. Transistors M1 through M4 constitute the high voltage switch which disconnects Vpp from the resistor when the device is not in the verify mode. The verify voltage generator includes a resistor divider and a buffer. Internal margin voltage generation maintains microprocessor compatibility by eliminating the need for external reference voltages.

Summary

Intel's ETOX Flash memory technology is a breakthrough in adding electrical chip-erasure to familiar EPROM technology. With cost-effective electrical erasure and reprogramming, Intel's 28F256 flash memory fills the functionality gap between traditional EPROMs and EEPROMs. EPROM-compatible specifications, straightforward interfacing, and in-circuit alterability allow designers to easily augment memory flexibility and satisfy the need for updatable code storage in today's designs.

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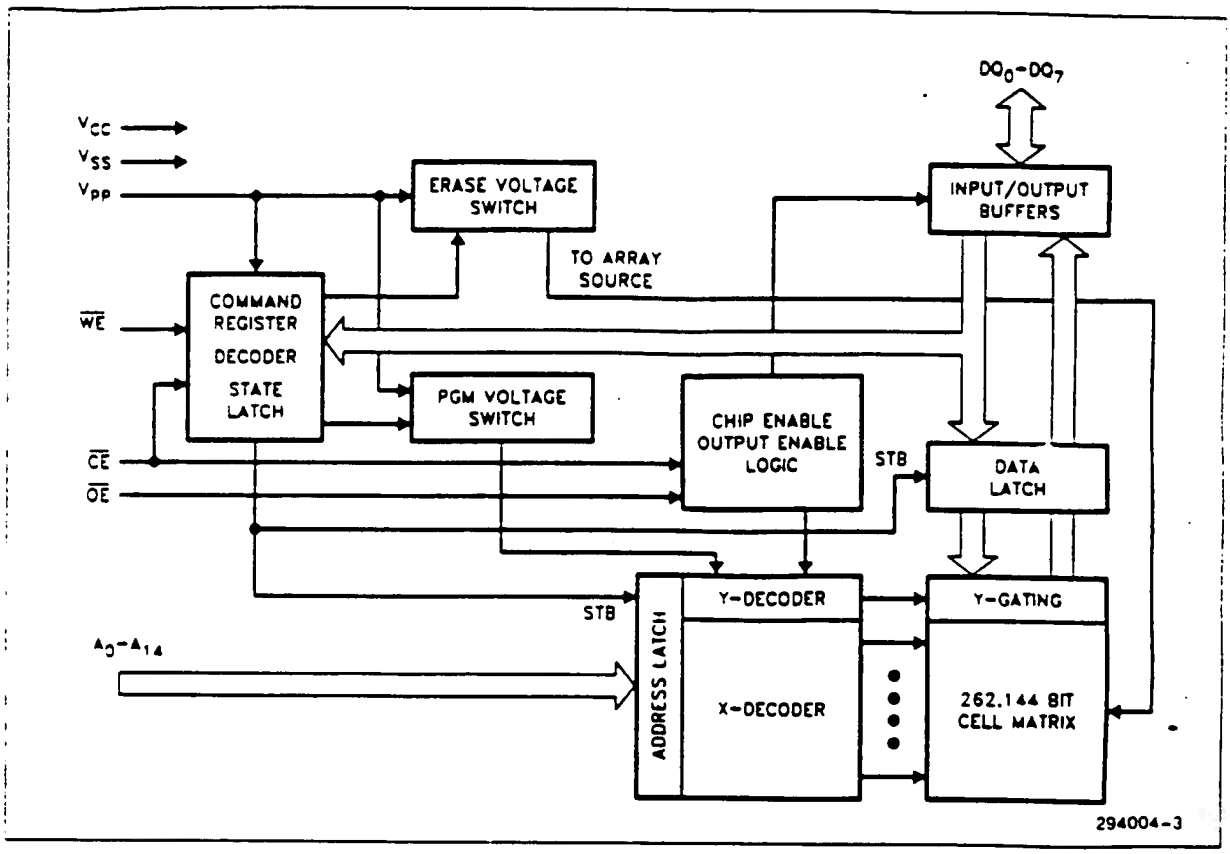


Figure 2. 28F256 Block Diagram

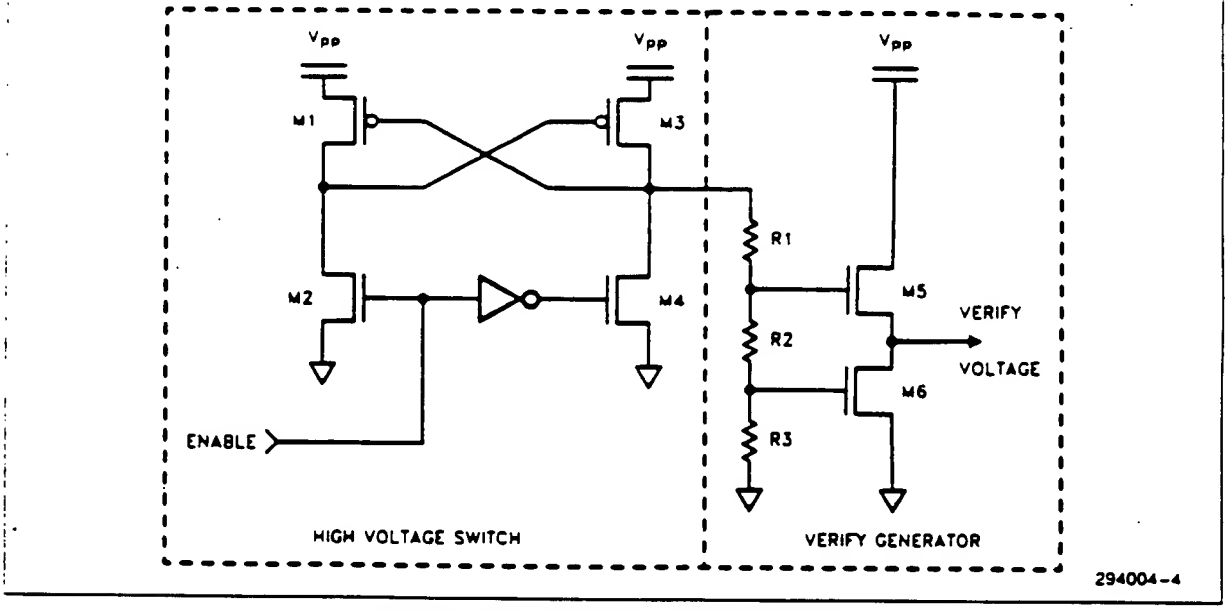


Figure 3. Erase/Program Verify Generator

SAN040100

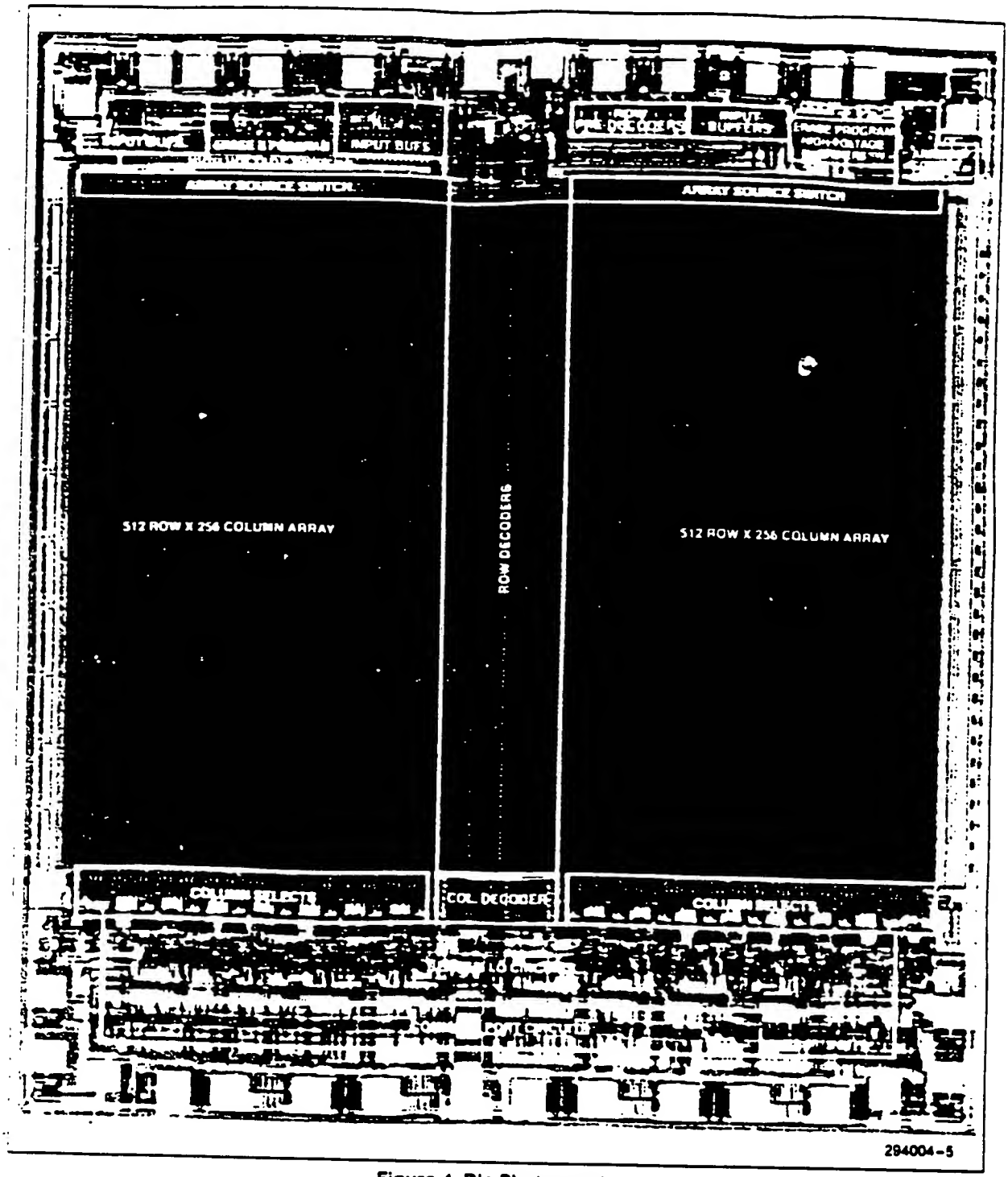
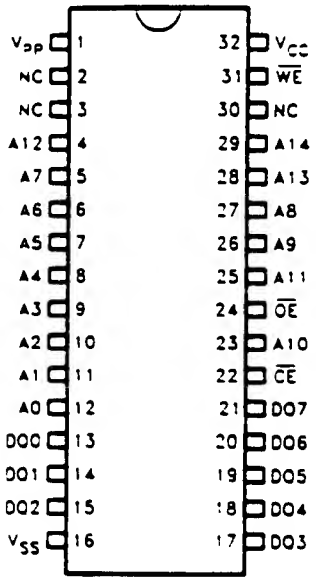


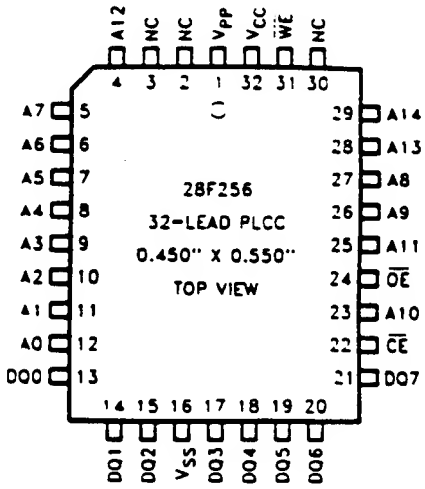
Figure 4. Die Photograph

SAN040101

28F256



294004-6



294004-7

Pin Names

A_0–A_{14}	Address Inputs
DQ_0–DQ_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{PP}	Program/Erase Power
V_{CC}	Device Power
V_{SS}	Ground

Figure 5. 28F256 Pin Configurations

SAN040102

Columns are numbered 0 through 255 beginning with the column nearest the X-decoder.

Quadrant Decoding (W)		Column Decoding (Y)				LEFT HALF ARRAY O0 O1 O2 O3		RIGHT HALF ARRAY O4 O5 O6 O7	
A4	A3	A2	A1	A0	A10	O0/O7	O1/O6	O2/O5	O3/O4
0	0	0	0	0	0	BL192	BL128	BL64	BL0
0	1	0	0	0	0	BL193	BL129	BL65	BL1
0	1	0	0	0	1	BL194	BL130	BL66	BL2
0	0	0	0	0	1	BL195	BL131	BL67	BL3
0	0	0	0	1	0	BL196	BL132	BL68	BL4
0	1	0	0	1	0	BL197	BL133	BL69	BL5
0	1	0	0	1	1	BL198	BL134	BL70	BL6
0	0	0	0	1	1	BL199	BL135	BL71	BL7
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	0	1	1	0	0	BL248	BL184	BL120	BL56
1	1	1	1	0	0	BL249	BL185	BL121	BL57
1	1	1	1	0	1	BL250	BL186	BL122	BL58
1	0	1	1	0	1	BL251	BL187	BL123	BL59
1	0	1	1	1	0	BL252	BL188	BL124	BL60
1	1	1	1	1	0	BL253	BL189	BL125	BL61
1	1	1	1	1	1	BL254	BL190	BL126	BL62
1	0	1	1	1	1	BL255	BL191	BL127	BL63

Figure 6. Bitline Decoding

SAN040103

X-DECODING. Wordlines are numbered 0 through 511 beginning at the top of the array.

WL	A14	A13	A12	A7	A6	A5	A11	A9	A8
WL0	0	0	0	0	0	0	0	0	0
WL1	0	0	0	0	0	0	0	0	1
WL2	0	0	0	0	0	0	0	1	0
WL3	0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
WL508	1	1	1	1	1	1	1	0	0
WL509	1	1	1	1	1	1	1	0	1
WL510	1	1	1	1	1	1	1	1	0
WL511	1	1	1	1	1	1	1	1	1

Figure 7. Wordline Decoding

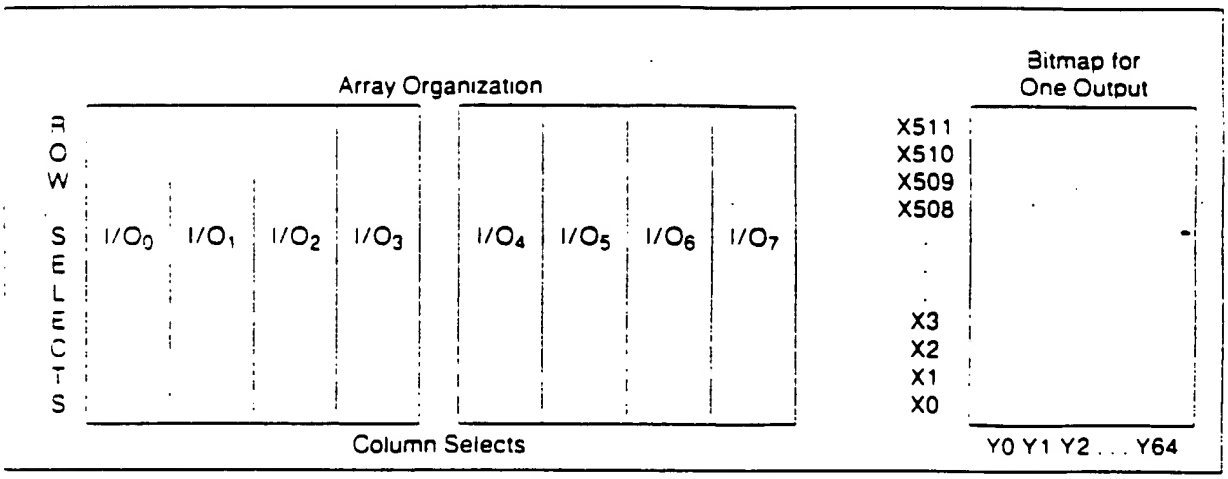


Figure 8. Bit Map

SAN040104

intel®

ENGINEERING REPORT

ER-23

October 1989

The Intel 28F512 Flash Memory

ENGINEERING REPORT

SAN040105

Order Number: 294007-002

INTRODUCTION

Intel's 28F512 ETOX™-II (EPROM tunnel oxide) flash memory adds electrical chip erasure and reprogramming to EPROM non-volatility and ease of use. Advances in tunnel oxides and photolithography have made it possible to develop a double-polysilicon single-transistor read/write random access nonvolatile memory, capable of greater than 10,000 reprogramming cycles. The 28F512 flash memory electrically erases all bits in the array matrix via electron tunneling. The EPROM programming mechanism of hot electron injection is employed for electrical byte programming.

A command port interface, internal margin voltage generation, and address and data latches augment standard EPROM circuitry to optimize Intel's 28F512 CMOS flash memory for microprocessor-controlled reprogramming.

Read timing parameters are equivalent to those of CMOS EPROMs, EEPROMs, and SRAMs. The 120 ns* access time results from a high memory cell current (95 μA), low resistance poly-silicide wordlines, advanced scaled periphery transistors, and an optimized data-out buffer.

The dense one-transistor cell structure, coupled with high array efficiency, yield a 512-kilobit die measuring 227 by 181 mils.

TECHNOLOGY OVERVIEW

Intel's ETOX-II flash memory technology is derived from its standard CMOS EPROM process base. Using advanced 1.0 μm double-polysilicon n-well CMOS technology, the 65,536 x 8-bit flash memory employs a 3.8 μm x 4.0 μm single transistor cell, affording equivalent array density as comparable EPROM technology. The flash memory cell structure is identical to the EPROM structure, except for the thinner gate (tunnel) oxide. Figure 1 compares the flash memory cell to the EPROM cell.

High quality tunnel oxide under the single floating polysilicon gate promotes electrical erasure. All cells in the array are simultaneously erased via Fowler-Nordheim tunneling. Applying 12V on the source junctions and grounding the select gates erases the entire array in one second (typical). Programming is accomplished with the standard EPROM mechanism of hot electron injection from the cell drain junction to the floating gate. Programming is initiated by bringing both the select gate and the cell drain to high voltage. Programming occurs at a typical rate of 10 μs per byte.

*Available 1H90

DEVICE ARCHITECTURE

Command Port

One feature which differentiates Intel's 512-kilobit flash memory is the command port architecture, illustrated in Figures 2 and 3.

The command port simplifies microprocessor control of the erase, erase verify, program, program verify, and read operations, without the need for additional control pins or the multiplexing of high voltage with control functions. On-chip address and data latches minimize system interface logic and free the system bus during erase and program operations. High voltage (12V) on the V_{PP} pin enables the command port. In the absence of this high voltage, the command port defaults to the read operation, inhibiting erasure or programming of the device.

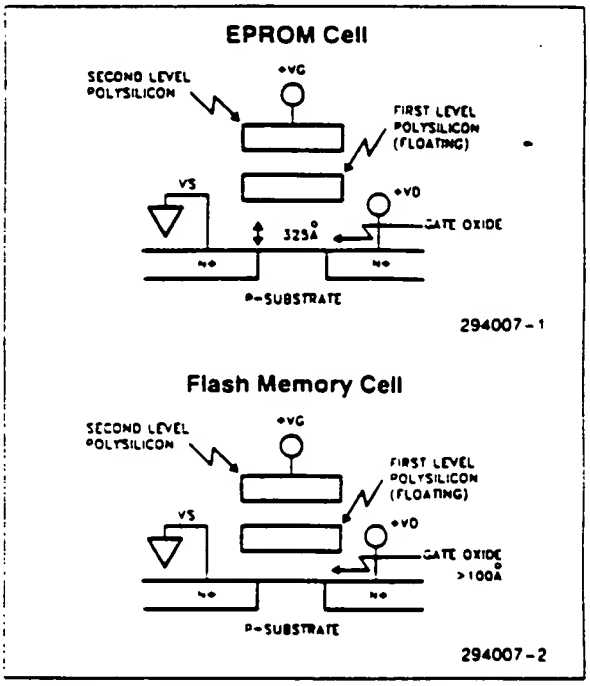


Figure 1. EPROM Cell vs. Flash Memory Cell

The command port consists of a command register, command decoder and state latch, the data-in latch, and the address latch. The command decoder output directs the operation of the high voltage flash-erase switch, program voltage generator, and the erase/program verify voltage generator.

Functions are selected via the command port in a microprocessor write cycle controlled by the Chip-Enable and Write-Enable pins. Contents of the address latch are updated on the falling edge of Write-Enable. The rising edge of Write-Enable latches the command and data registers, and initiates operations.

Erasure

Erasure is achieved through a two-step write sequence. The erase set-up code is written to the command register in the first cycle. The erase confirmation code is written in the second cycle. The rising edge of this second Write-Enable pulse initiates the erase operation. The command decoder triggers the high voltage flash-erase switch, connecting the 12V supply to the source of all bits in the array, while all wordlines are grounded. Fowler-Nordheim tunneling results in the simultaneous erasure of all bits.

The array source switch, shown in Figure 4, switches high voltage onto the source junctions. During erasure, the high voltage latch formed by M5 through M8 enables transistor M15. Transistor M15 pulls the array source up to 12V. Transistor M16 pulls the source to ground during read and program operations.

To obtain fast erase times, the device must supply the grounded gate breakdown current which occurs on the sources of the memory array. The upper boundary for current sourcing capability of M15 is set by the maximum allowable substrate current. If V_{PP} is raised to 12V before V_{CC} is above approximately 1.8V, the low V_{CC} detect circuit formed by transistors M1 to M4 drives the node LOW V_{CC} to 9V. Transistors M9 to M11 then force the erase circuit into a non-erase state with M15 off and M16 on. When V_{CC} rises above 1.8V, the chip will be reset into the read state.

Writing the erase verify code into the command register terminates erasure, latches the address of the byte to verify, and sets the internally-generated erase margin voltage. The microprocessor then accesses the output from the addressed byte using standard read timings. The verify procedure repeats for all addresses. Should a byte require more time to reach the erased state, another erase operation is applied. The erase and verify operations continue until the entire array is erased.

Programming

Programming follows a similar flow. The program set-up command is written to the command register on the first cycle. The second cycle loads the address and data latches. The rising edge of the second Write-Enable pulse initiates programming by applying high voltage to the gates and drains of the bits to be programmed.

Writing the program verify command to the register terminates the programming operation and applies the program verify voltage to the newly programmed byte. Again, the addressed byte can be read using standard microprocessor read timings. Should the addressed byte require more time to reach the programmed state, the programming operation and verification are repeated until the byte is programmed.

DEVICE RELIABILITY

Cell Margining

Erase and program verification ensure the data retention of the newly altered memory bits. The cell margining performed in the Quick-Pulse Programming™ and Quick-Erase™ algorithms is more reliable than historical overpulsing schemes as margining tests the amount of charge stored on the floating gate.

Intel's flash memories employ a unique circuit to internally generate the erase and program verify voltages. Figure 5 shows a simplified version of the circuit. The circuit consists of a high voltage switch and the verify voltage generator. Transistors M1 through M4 constitute the high voltage switch which disconnects V_{PP} from the resistor when the device is not in the verify mode. The verify voltage generator includes a resistor divider and a buffer. Internal margin voltage generation maintains microprocessor compatibility by eliminating the need for external reference voltages.

Erase/Program Cycling

One of the most significant aspects of the 28F512 is its capability for a minimum of 10,000 erase/program cycles. Destructive oxide breakdown has been a limiting factor in extended cycling of thin oxide EEPROMs. Intel's ETOX-II flash memory technology extends cycling performance through: improved tunnel oxide processing that increases charge carrying capability tenfold; reduced oxide area under stress minimizing probability of oxide defects in the region; and reduced oxide stress due to a lower peak electric field (lower erase voltage than EEPROM).

A typical cell erase/program margin (Vt) is shown as a function of reprogramming cycles in Figure 6. After 10,000 reprogramming cycles, a 2.5V program read margin exists, ensuring reliable data retention. Accelerated retention bake experiments, for devices with 10,000 reprogramming cycles, show minimal program Vt shift.

Reliable erase/program cycling also requires proper selection of the erase Vt maximum and maintenance of a tight Vt distribution. The maximum erase Vt is set to 3.2V via the erase algorithm and the internal erase verify circuits. Superior oxide quality gives an erase Vt distribution width that improves slightly with cycling (Figure 7). The tight erased Vt distribution gives an order of magnitude of erase time margin to the fastest erasing cell (Figure 8).

Figures 9 and 10 illustrate typical programming performance over variations in temperature and V_{PP}. Figures 11 and 12 depict typical erase performance versus temperature and V_{PP}. As seen in these figures, the 28F512 performs extended erase and program cycling well within the performance boundaries of the program and erase algorithms.

SUMMARY

Intel's ETOX-II flash memory technology is a breakthrough in adding electrical chip-erasure to high-density EPROM technology. Intel's 28F512 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. Microprocessor-compatible specifications, straightforward interfacing, and in-circuit alterability allow designers to easily augment memory flexibility and satisfy the need for nonvolatile storage in today's designs.

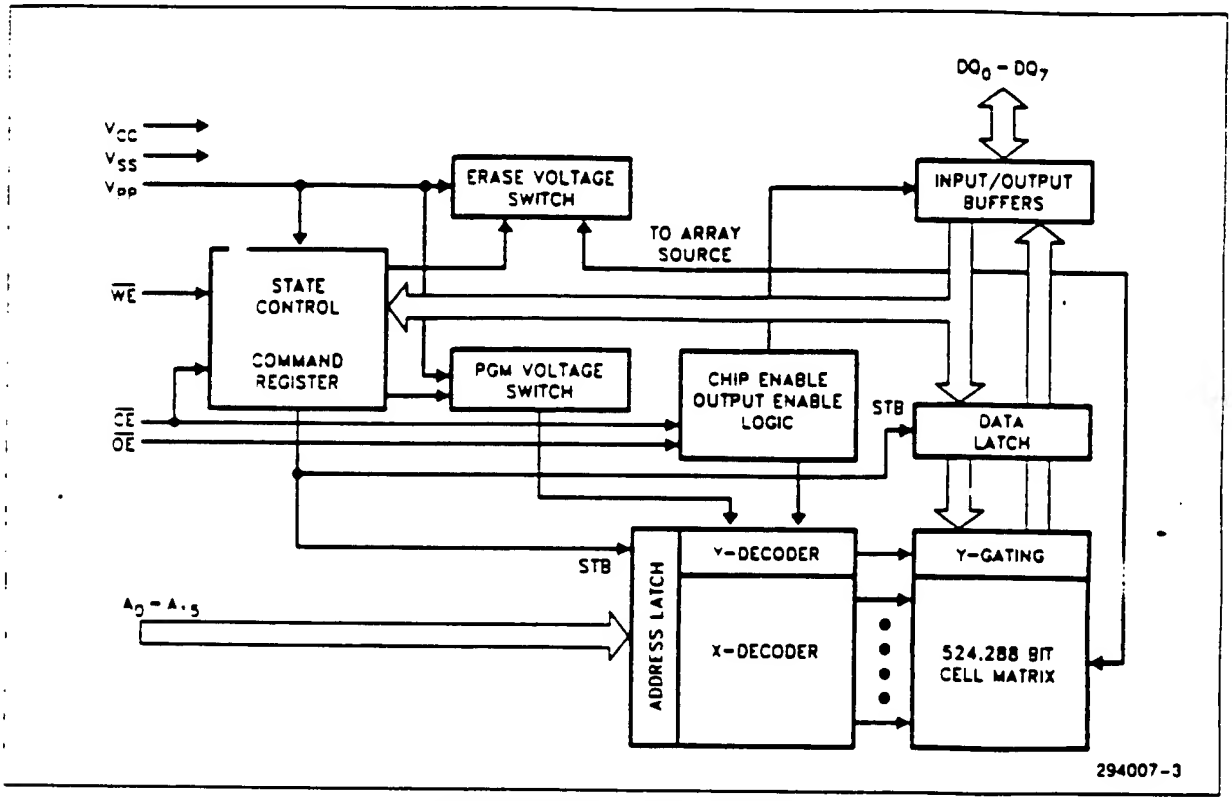


Figure 2. 28F512 Block Diagram

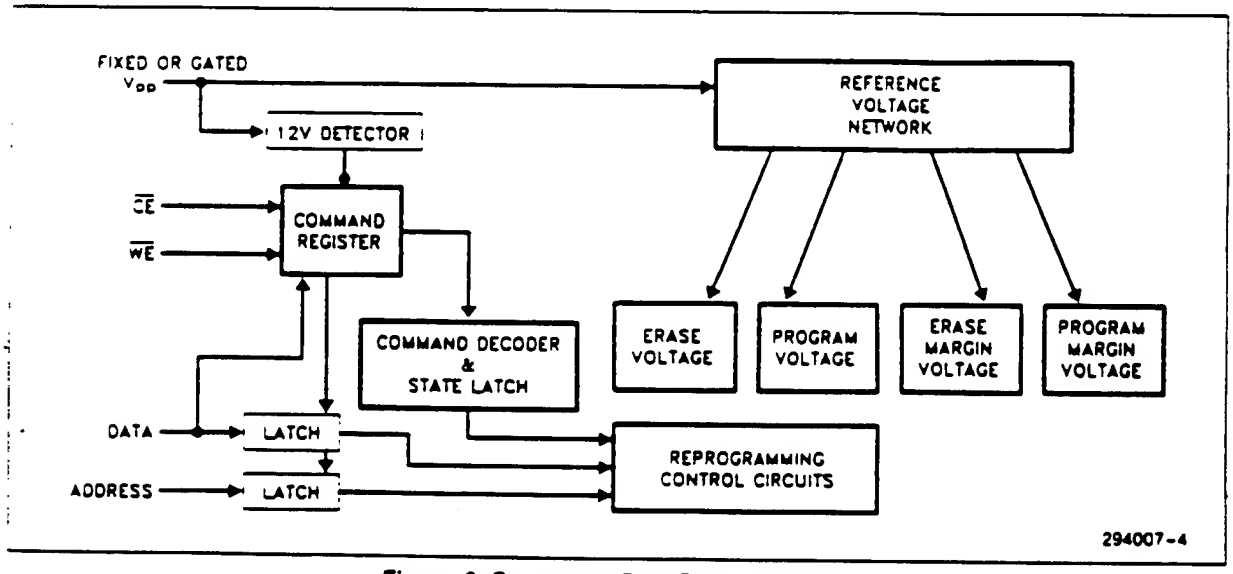


Figure 3. Command Port Block Diagram

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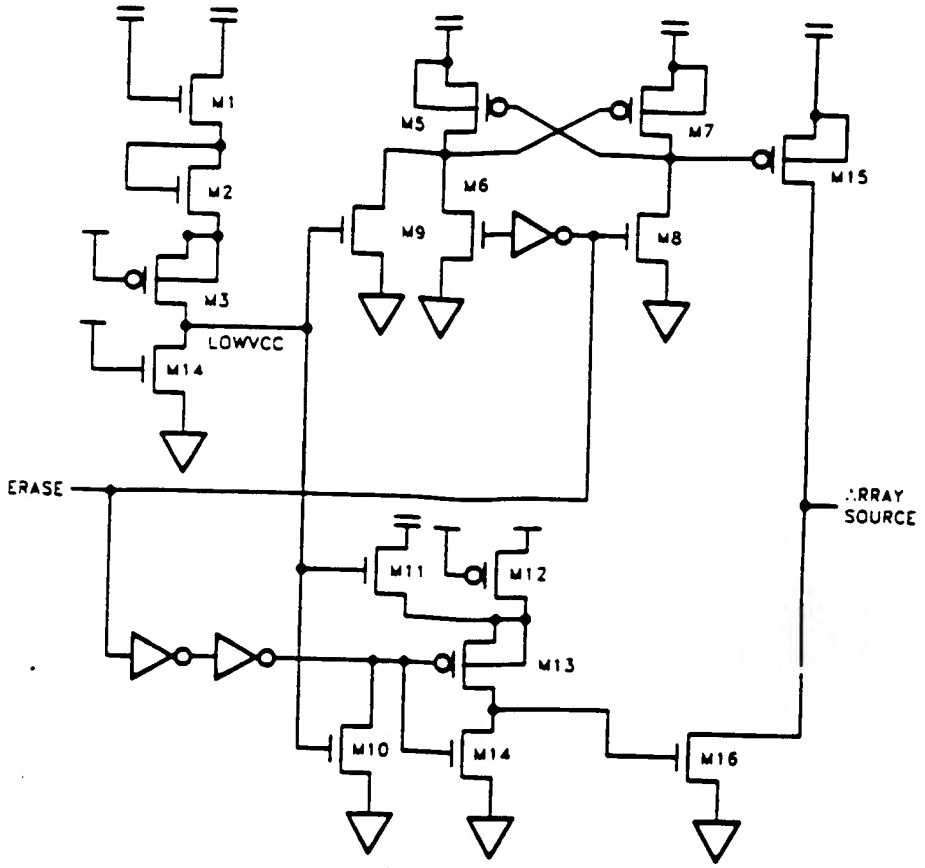

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Figure 4. Array Source Switch

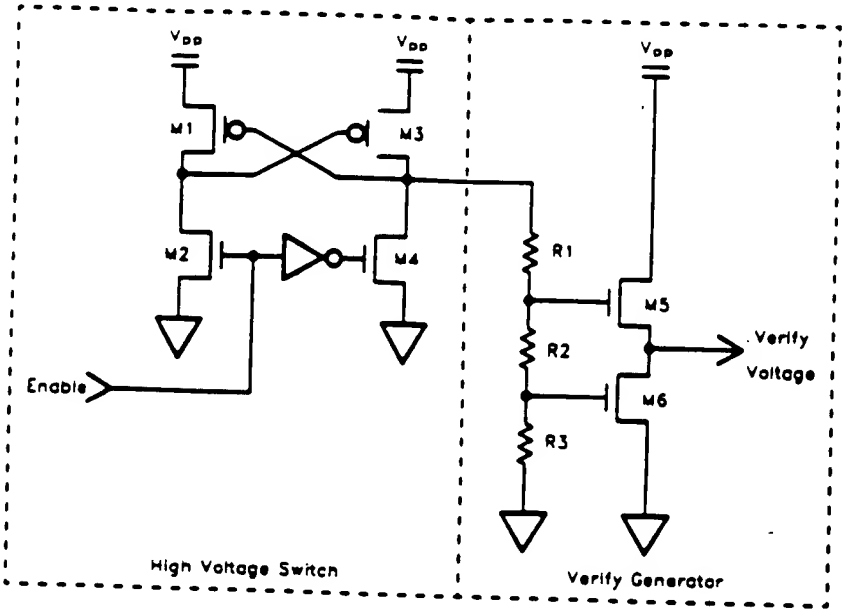

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Figure 5. Erase/Program Verify Generator

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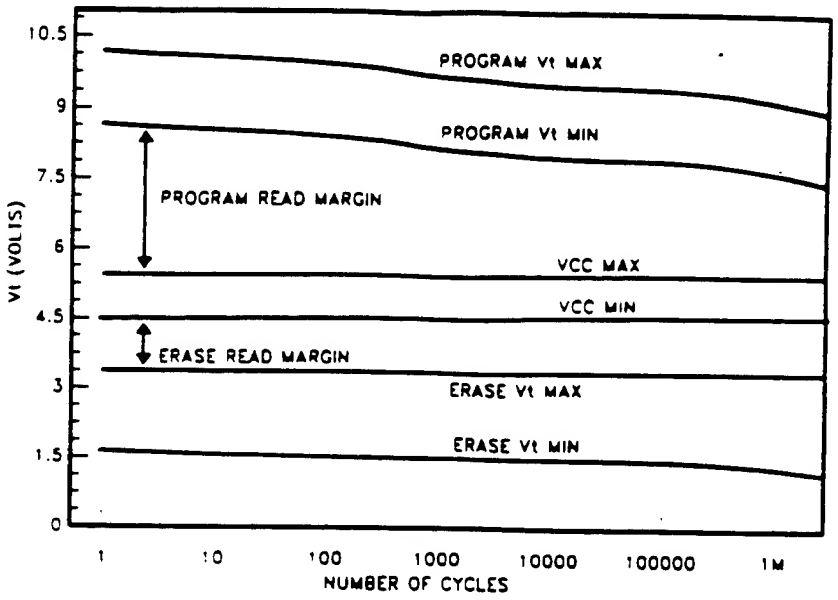

Figure 6. Array Vt vs. Cycles

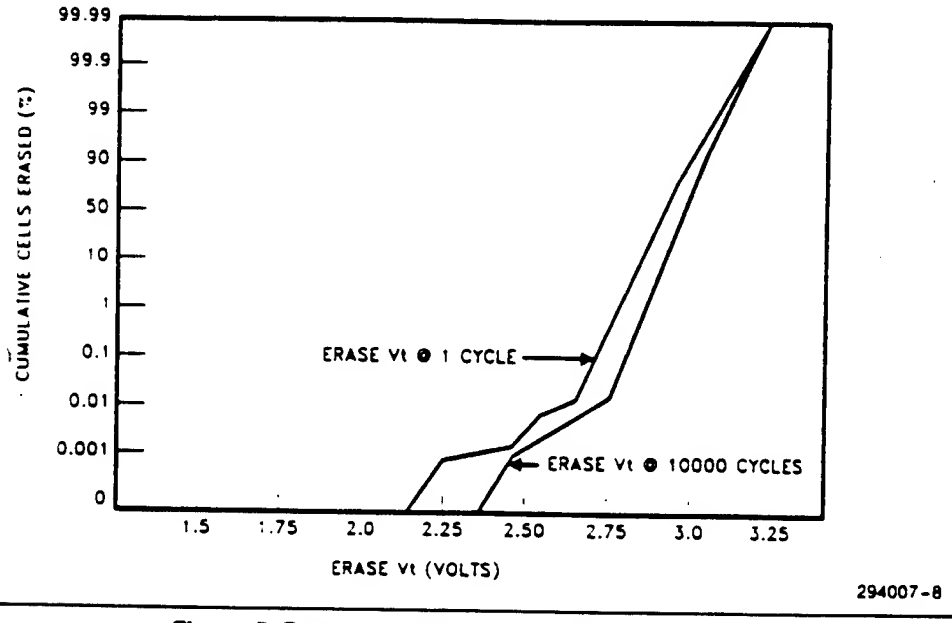

Figure 7. Erase Vt Distribution vs. Cycling

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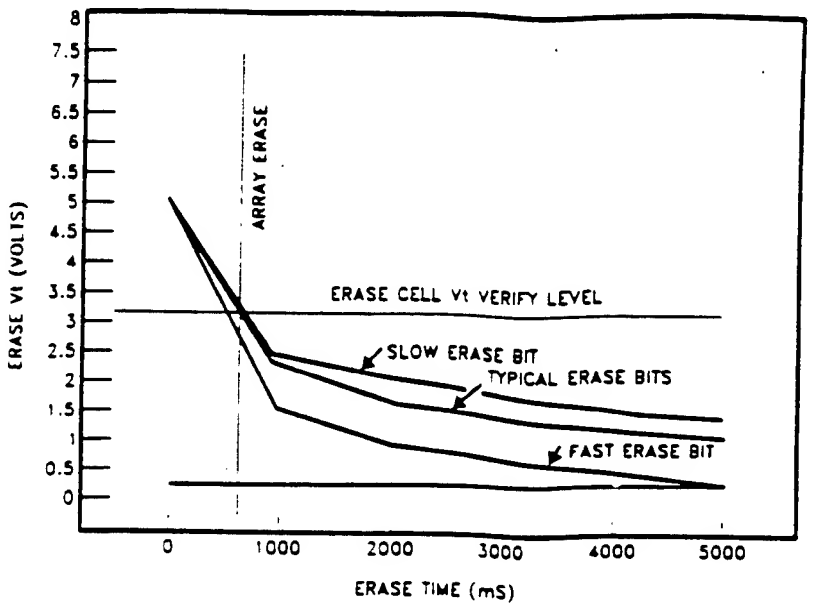

Figure 8. Array Erase Vt vs. Erase Time

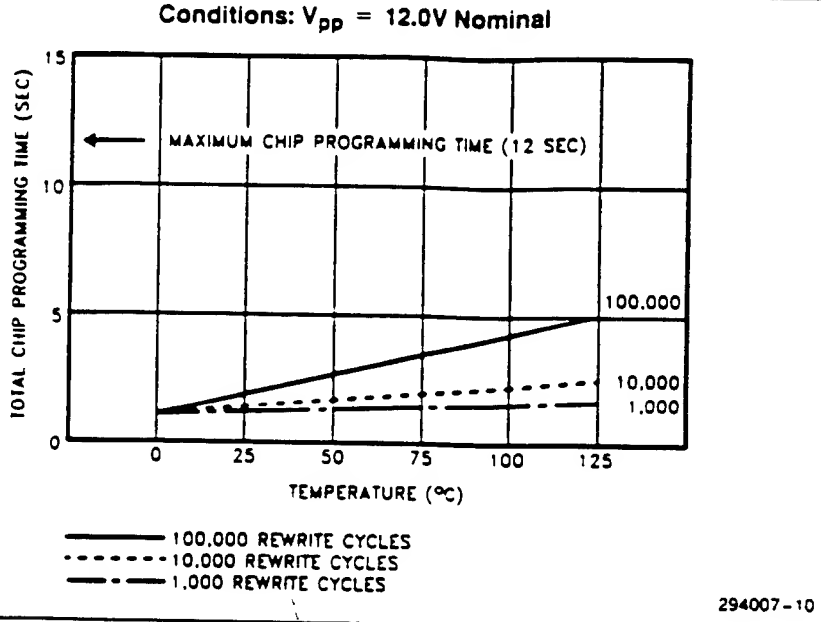

Figure 9. 28F512 Typical Programming Time vs. Temperature

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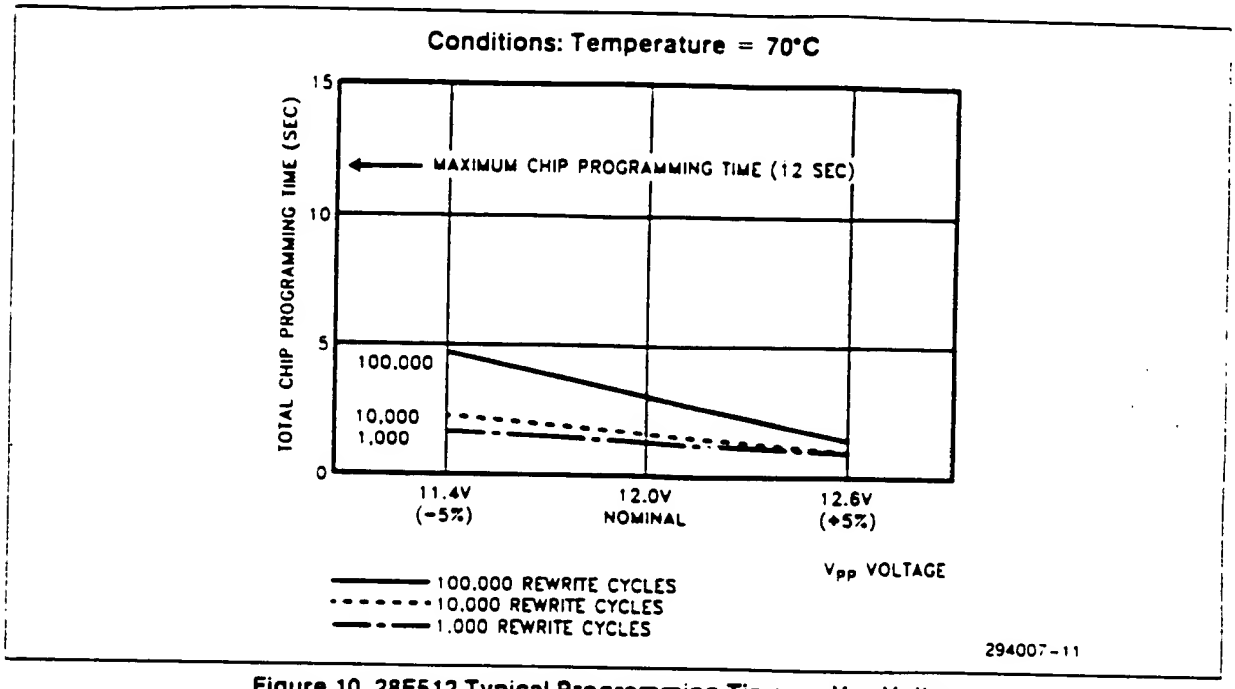

Figure 10. 28F512 Typical Programming Time vs. V_{PP} Voltage

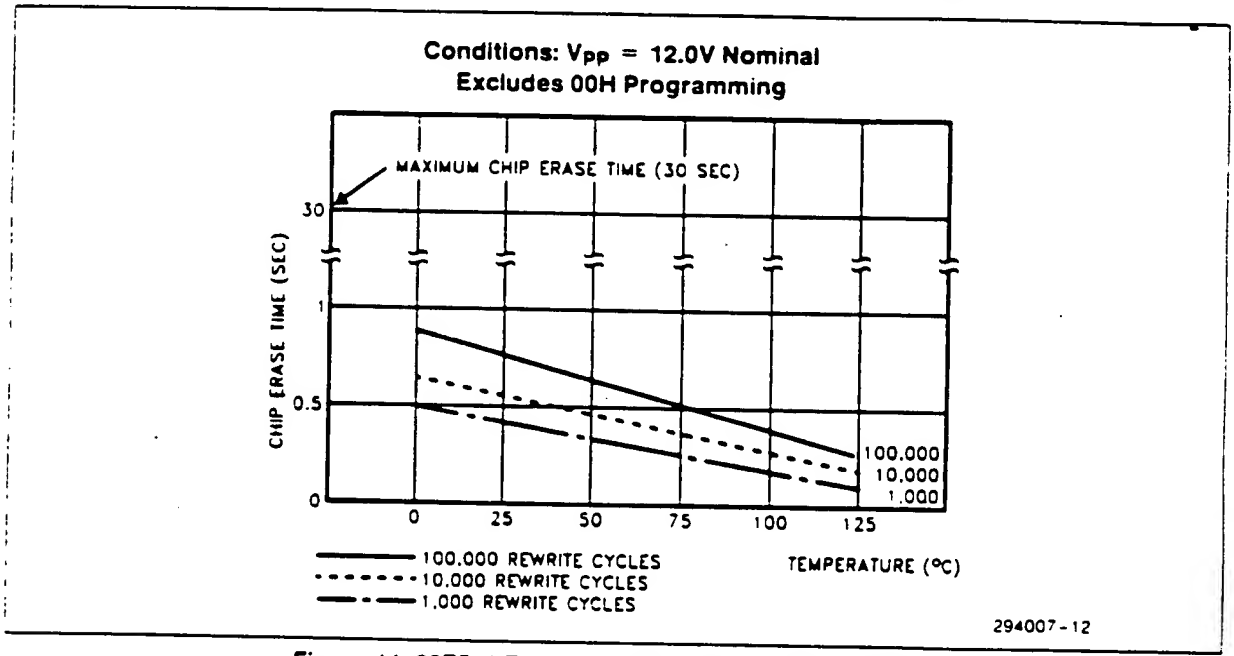

Figure 11. 28F512 Typical Erase Time vs. Temperature

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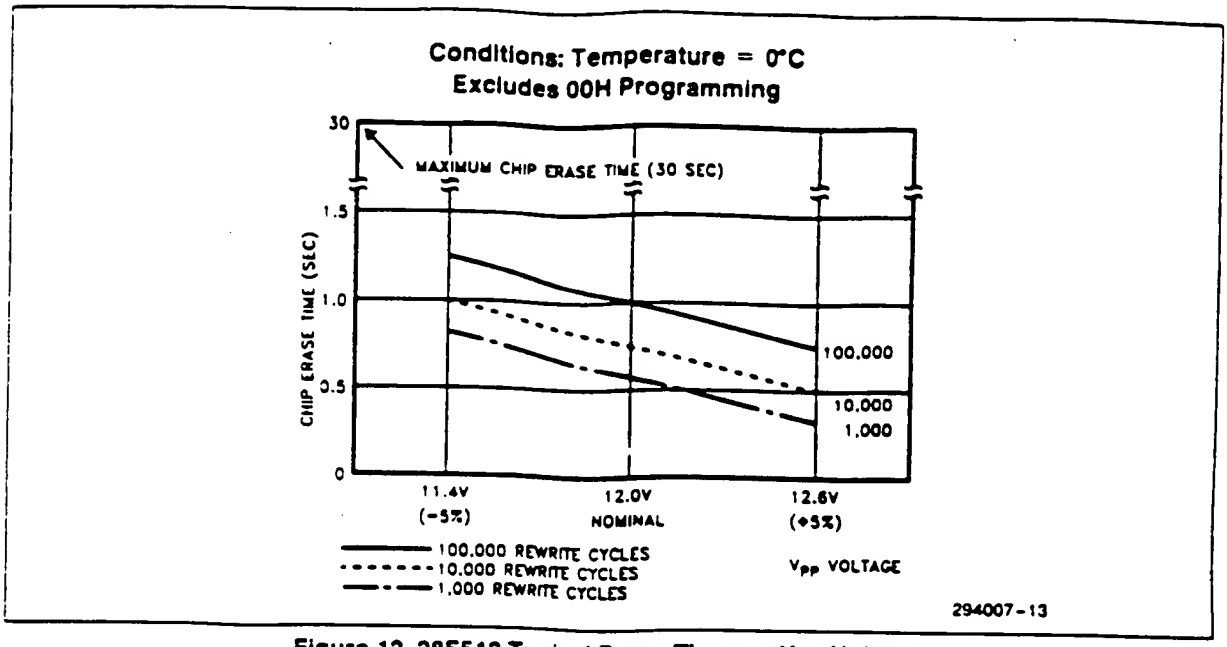

Figure 12. 28F512 Typical Erase Time vs. V_{PP} Voltage

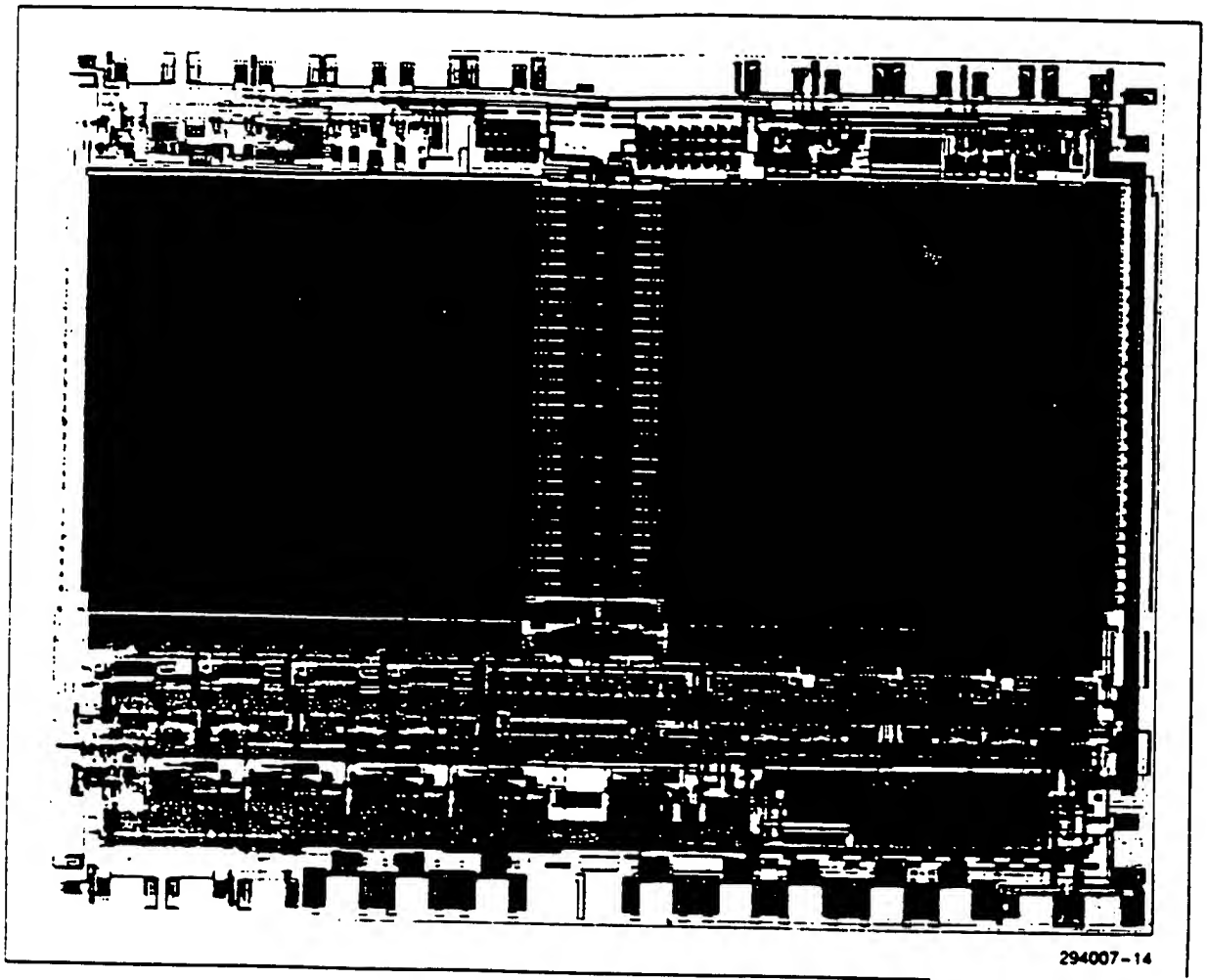

Figure 13. 28F512 Die Photograph

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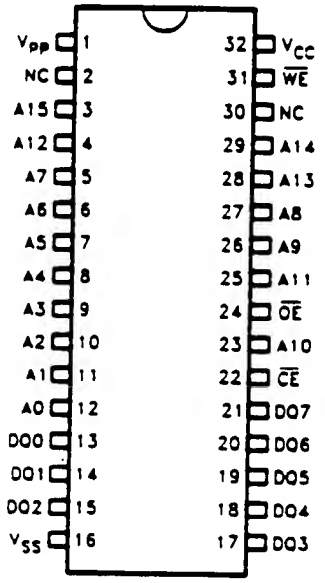
28F512



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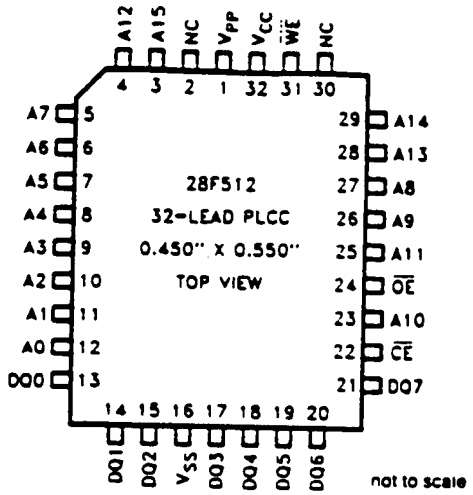

not to scale

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Pin Names

A_0–A_{15}	Address Inputs
DQ_0–DQ_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{PP}	Program/Erase Power
V_{CC}	Device Power
V_{SS}	Ground

Figure 14. 28F512 Pin Configurations

SAN040114

Columns are numbered 0 through 511 beginning with the column nearest the X-decoder.

Outputs are grouped as follows:

							Left Half Array O0 O1		Right Half Array O4 O5	O6 O7
Address							Bitlines			
A14	A15	A3	A10	A2	A1	A0	IO0/7	IO1/06	IO2/05	IO3/04
0	0	0	0	0	0	0	BL384	BL256	BL128	BL0
0	0	1	0	0	0	0	BL385	BL257	BL129	BL1
0	0	0	0	0	0	1	BL386	BL258	BL130	BL2
0	0	1	0	0	0	1	BL387	BL259	BL131	BL3
0	0	0	0	0	1	0	BL388	BL260	BL132	BL4
0	0	1	0	0	1	0	BL389	BL261	BL133	BL5
0	0	0	0	0	1	1	BL390	BL262	BL134	BL6
0	0	1	0	0	1	1	BL391	BL263	BL135	BL7
•	•	•	•	•	•	•	•	•	•	•
1	1	0	1	1	1	0	BL508	BL380	BL252	BL124
1	1	1	1	1	1	0	BL509	BL381	BL253	BL125
1	1	0	1	1	1	1	BL510	BL382	BL254	BL126
1	1	1	1	1	1	1	BL511	BL383	BL255	BL127

Figure 15. Bitline Decoding

X-DECODING: Wordlines are numbered 0 through 511 beginning at the top of the array.

X Address									Row
A12	A7	A6	A5	A4	A13	A11	A9	A8	WL
0	0	0	0	0	0	0	0	0	XL0
0	0	0	0	0	0	0	0	1	XL1
0	0	0	0	0	0	0	1	0	XL2
0	0	0	0	0	0	0	1	1	XL3
0	0	0	0	0	0	1	0	0	XL4
0	0	0	0	0	0	1	0	1	XL5
0	0	0	0	0	0	1	1	0	XL6
0	0	0	0	0	0	1	1	1	XL7
0	0	0	0	0	1	0	0	0	XL8
0	0	0	0	0	1	0	0	1	XL9
0	0	0	0	0	1	0	1	0	XL10
0	0	0	0	0	1	0	1	1	XL11
0	0	0	0	0	1	1	0	0	XL12
0	0	0	0	0	1	1	0	1	XL13
0	0	0	0	0	1	1	1	0	XL14
0	0	0	0	0	1	1	1	1	XL15
0	0	0	0	1	1	1	1	1	XL16
0	0	0	0	1	1	1	1	0	XL17
0	0	0	0	1	1	1	0	1	XL18
0	0	0	0	1	1	1	0	0	XL19
0	0	0	0	1	1	0	1	1	XL20
0	0	0	0	1	1	0	1	0	XL21
0	0	0	0	1	1	0	0	1	XL22
0	0	0	0	1	1	0	0	0	XL23
0	0	0	0	1	0	1	1	1	XL24
0	0	0	0	1	0	1	1	0	XL25
0	0	0	0	1	0	1	0	1	XL26
0	0	0	0	1	0	1	0	0	XL27
0	0	0	0	1	0	0	1	1	XL28
0	0	0	0	1	0	0	1	0	XL29
0	0	0	0	1	0	0	0	1	XL30
0	0	0	0	1	0	0	0	0	XL31

Figure 16. Wordline Decoding (Continued)

X-DECODING: Wordlines are number 0 through 511 beginning at the top of the array.

X Address									Row
A12	A7	A6	A5	A4	A13	A11	A9	A8	WL
0	0	0	1	0	0	0	0	0	XL32
•	•	•	•	•	•	•	•	•	•
0	0	0	1	0	1	1	1	1	XL47
0	0	0	1	1	1	1	1	1	XL48
•	•	•	•	•	•	•	•	•	•
0	0	0	1	1	0	0	0	0	XL63
0	0	1	0	0	0	0	0	0	XL64
•	•	•	•	•	•	•	•	•	•
0	0	1	0	0	1	1	1	1	XL79
0	0	1	0	1	1	1	1	1	XL80
•	•	•	•	•	•	•	•	•	•
0	0	1	0	1	0	0	0	0	XL95
1	1	1	1	0	0	0	0	0	XL480
•	•	•	•	•	•	•	•	•	•
1	1	1	1	0	1	1	1	1	XL495
1	1	1	1	1	1	1	1	1	XL496
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	0	0	0	0	XL511

Figure 16. Wordline Decoding (Continued)

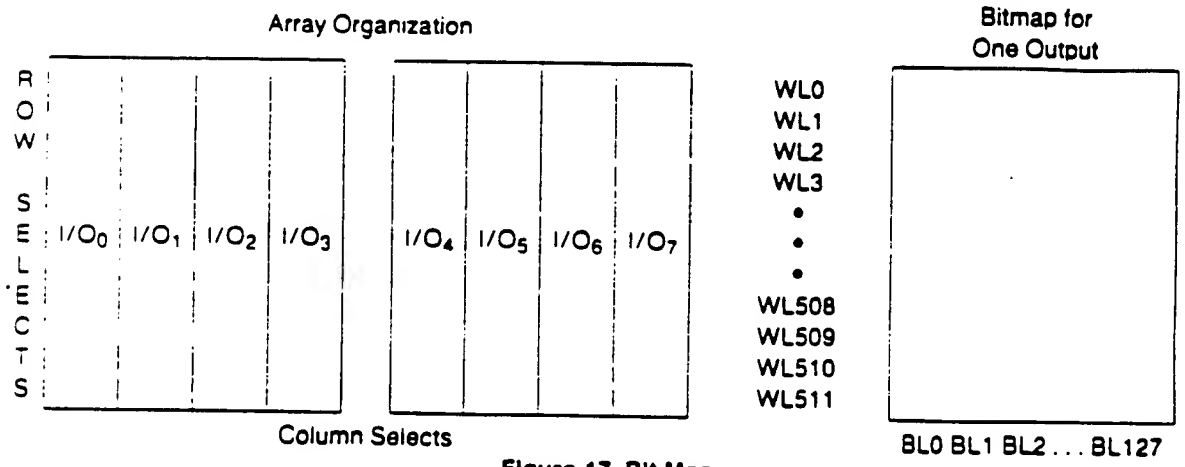


Figure 17. Bit Map

SAN040116

intel®

ENGINEERING REPORT

ER-24

October 1989

The Intel 28F010 Flash Memory

SAN040117

Order Number: 294008-003

INTRODUCTION

Intel's 28F010 ETOX™-II (EPROM tunnel oxide) flash memory adds electrical chip erasure and reprogramming to EPROM non-volatility and ease of use. Advances in tunnel oxides and photolithography have made it possible to develop a double-polysilicon single-transistor read/write random access nonvolatile memory, capable of greater than 10,000 reprogramming cycles. The 28F010 flash memory electrically erases all bits in the array matrix via electron tunneling. The EPROM programming mechanism of hot electron injection is employed for electrical byte programming.

A command port interface, internal margin voltage generation, and address and data latches augment standard EPROM circuitry to make Intel's 28F010 the highest density CMOS flash memory for microprocessor-controlled reprogramming.

Read timing parameters are equivalent to those of CMOS EPROMs, EEPROMs, and SRAMs. The 135 ns access time results from a high memory cell current (95 μA), low resistance poly-silicide wordlines, advanced scaled periphery transistors, and an optimized data-out buffer.

The dense one-transistor cell structure, coupled with high array efficiency, yields a one megabit die measuring 225 by 265 mils.

TECHNOLOGY OVERVIEW

Intel's ETOX-II flash memory technology is derived from its standard CMOS EPROM process base. Using advanced 1.0 μm double-polysilicon n-well CMOS technology, the 131,072 x 8 bit flash memory employs a 3.8 μm x 4.0 μm single transistor cell, affording equivalent array density as comparable EPROM technology. The flash memory cell structure is identical to the EPROM structure, except for the thinner gate (tunnel) oxide. Figure 1 compares the flash memory cell to the EPROM cell.

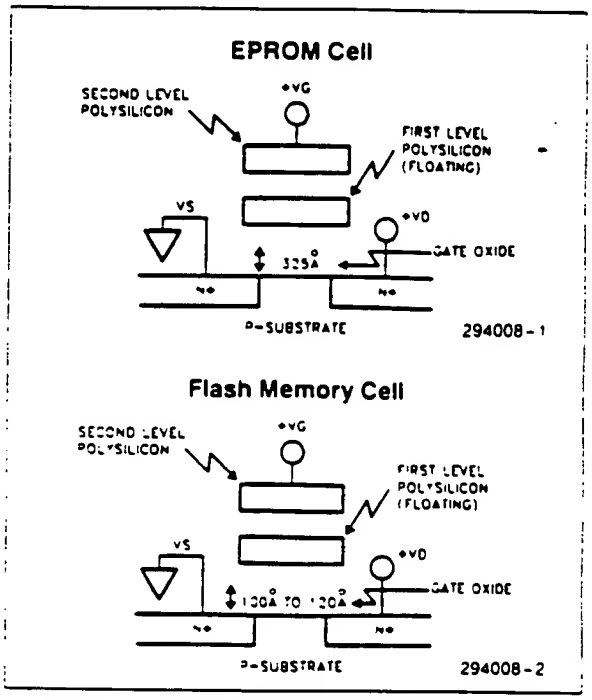
High quality tunnel oxide under the single floating polysilicon gate promotes electrical erasure. All cells in the array are simultaneously erased via Fowler-Nordheim tunneling. Applying 12V on the source junctions and grounding the select gates erases the entire array in two seconds (typical). Programming is accomplished with the standard EPROM mechanism of hot electron injection from the cell drain junction to the floating gate. Programming is initiated by bringing both the select gate and the cell drain to high voltage. Programming occurs at a rate of 10 μs per byte.

DEVICE ARCHITECTURE

Command Port

One feature which differentiates Intel's one-megabit flash memory is the command port architecture, illustrated in Figures 2 and 3.

The command port simplifies microprocessor control of the erase, erase verify, program, program verify, and read operations, without the need for additional control pins or the multiplexing of high voltage with control functions. On-chip address and data latches minimize system interface logic and free the system bus during erase and program operations. High voltage (12V) on the V_{PP} pin enables the command port. In the absence of this high voltage, the command port defaults to the read operation, inhibiting erasure or programming of the device.



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The command port consists of a command register, command decoder and state latch, the data-in latch, and the address latch. The command decoder output directs the operation of the high voltage flash-erase switch, program voltage generator, and the erase/program verify voltage generator

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Erasure

Erasure is achieved through a two-step write sequence. The erase set-up code is written to the command register in the first cycle. The erase confirmation code is written in the second cycle. The rising edge of this second Write-Enable pulse initiates the erase operation. The command decoder triggers the high voltage flash-erase switch, connecting the 12V supply to the source of all bits in the array, while all wordlines are grounded. Fowler-Nordheim tunneling results in the simultaneous erasure of all bits.

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Writing the erase verify code into the command register terminates erasure, latches the address of the byte to verify, and sets the internally-generated erase margin voltage. The microprocessor then accesses the output from the addressed byte using standard read timings. The verify procedure repeats for all addresses. Should a byte require more time to reach the erased state, another erase operation is applied. The erase and verify operations continue until the entire array is erased.

Programming

Programming follows a similar flow. The program set-up command is written to the command register on the first cycle. The second cycle loads the address and data latches. The rising edge of the second Write-Enable pulse initiates programming by applying high voltage to the gates and drains of the bits to be programmed.

Writing the program verify command to the register terminates the programming operation and applies the program verify voltage to the newly programmed byte. Again, the addressed byte can be read using standard microprocessor read timings. Should the addressed byte require more time to reach the programmed state, the programming operation and verification are repeated until the byte is programmed.

DEVICE RELIABILITY

Cell Margining

Erase and program verification ensure the data retention of the newly altered memory bits. The cell margining performed in the Quick-Pulse Programming™ and Quick-Erase™ algorithms is more reliable than historical overpulsing schemes as margining tests the amount of charge stored on the floating gate.

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A typical cell erase/program margin (Vt) is shown as a function of reprogramming cycles in Figure 6. After 10,000 reprogramming cycles, a 2.5V program read margin exists, ensuring reliable data retention. Accelerated retention bake experiments, for devices with 10,000 reprogramming cycles, show minimal program Vt shift.

Reliable erase/program cycling also requires proper selection of the erase Vt maximum and maintenance of a tight Vt distribution. The maximum erased Vt is set to 3.2V via the erase algorithm and the internal erase verify circuits. Superior oxide quality gives an erased Vt distribution width that improves slightly with cycling (Figure 7). The tight erase Vt distribution gives an order of magnitude of erase time margin to the fastest erasing cell (Figure 8).

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Figures 9 and 10 illustrate typical programming performance over variations in temperature and V_{PP}. Figures 11 and 12 depict typical erase performance versus temperature and V_{PP}. As seen in these figures, the 28F010 performs extended erase and program cycling well within the performance boundaries of the program and erase algorithms.

SUMMARY

Intel's ETOX-II flash memory technology is a breakthrough in adding electrical chip-erasure to high-density EPROM technology. Intel's 28F010 CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access non-volatile memory. Microprocessor-compatible specifications, straightforward interfacing, and in circuit alterability allow designers to easily augment memory flexibility and satisfy the need for nonvolatile storage in today's designs.

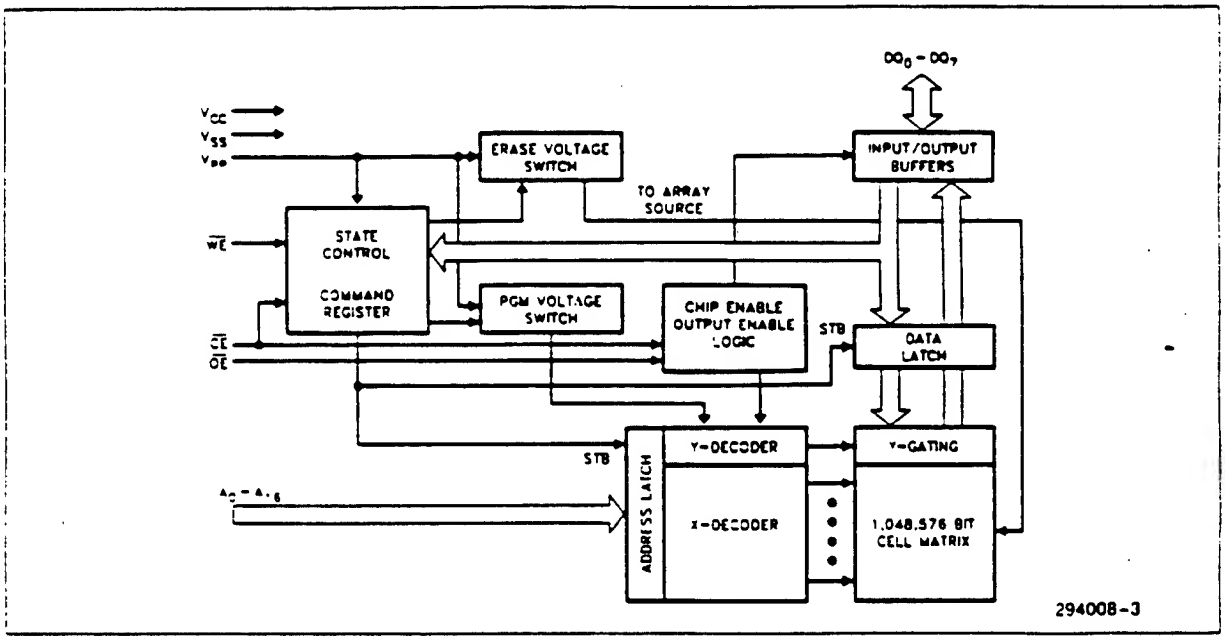

Figure 2. 28F010 Block Diagram

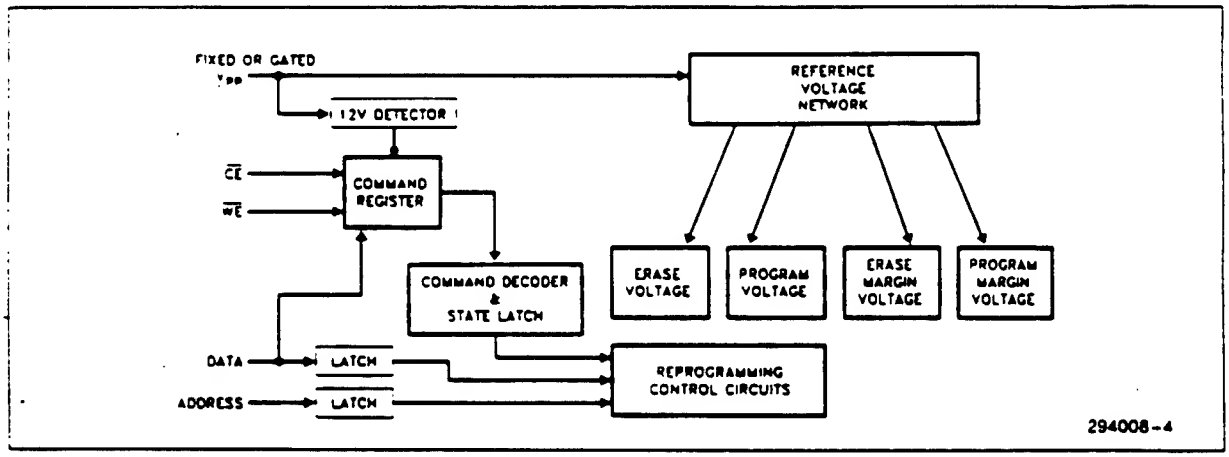

Figure 3. Command Port Block Diagram

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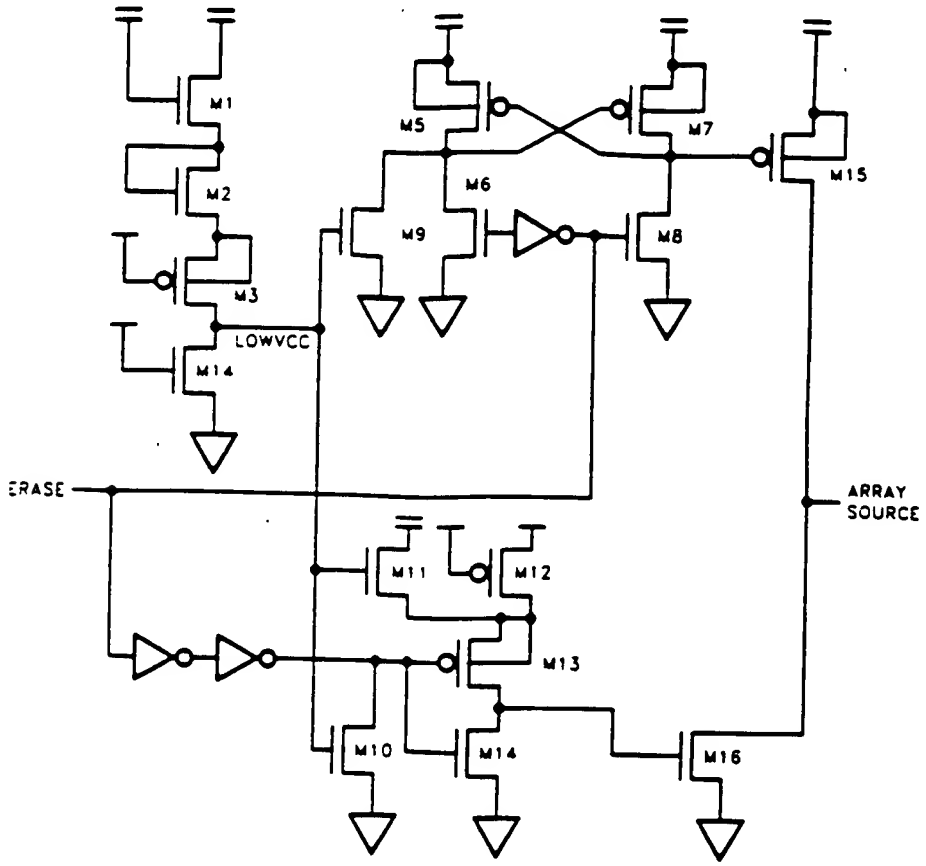

Figure 4. Array Source Switch

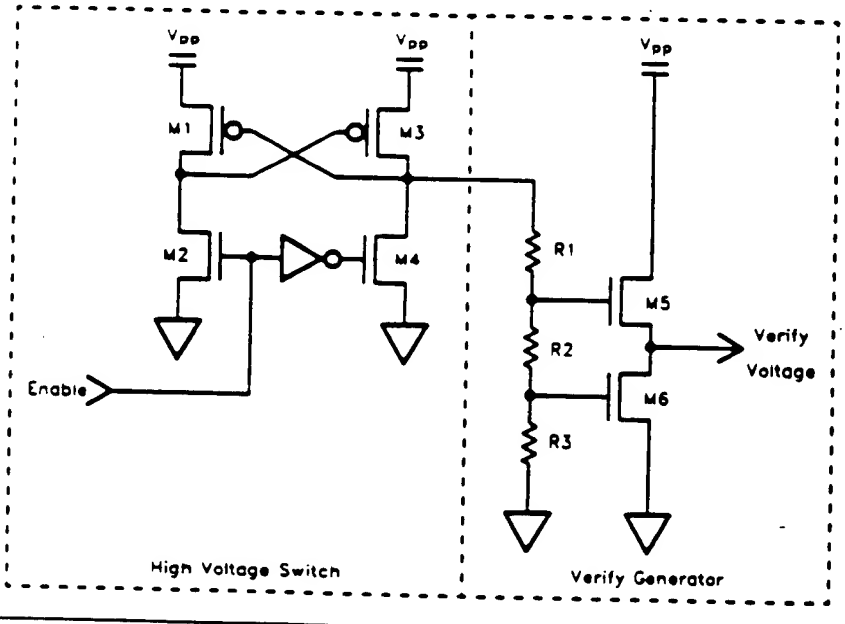

Figure 5. Erase/Program Verify Generator

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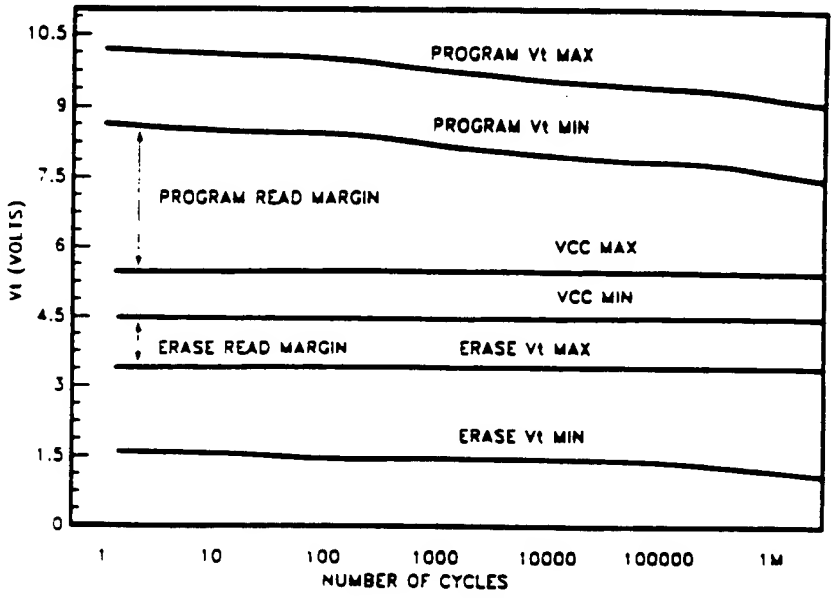

Figure 6. 1M Array VT vs. Cycles

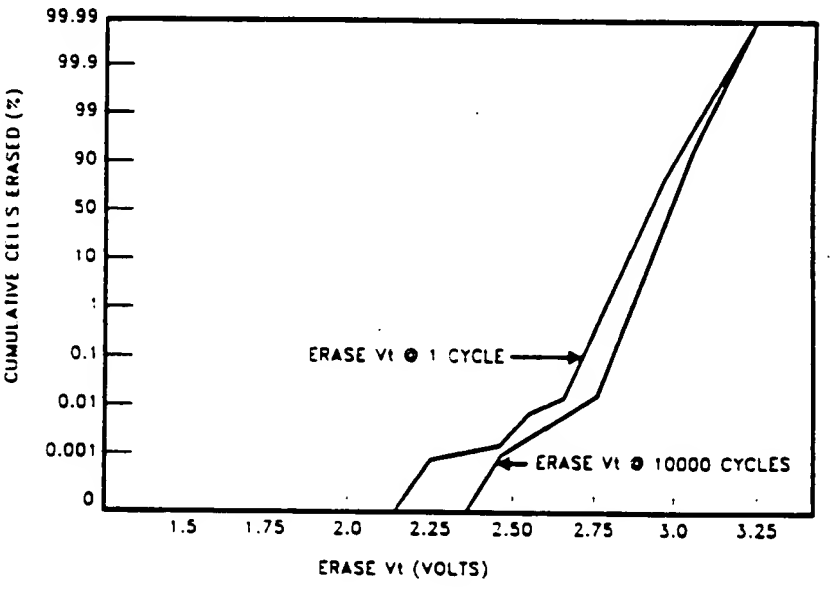

Figure 7. Erase Vt Distribution vs. Cycling

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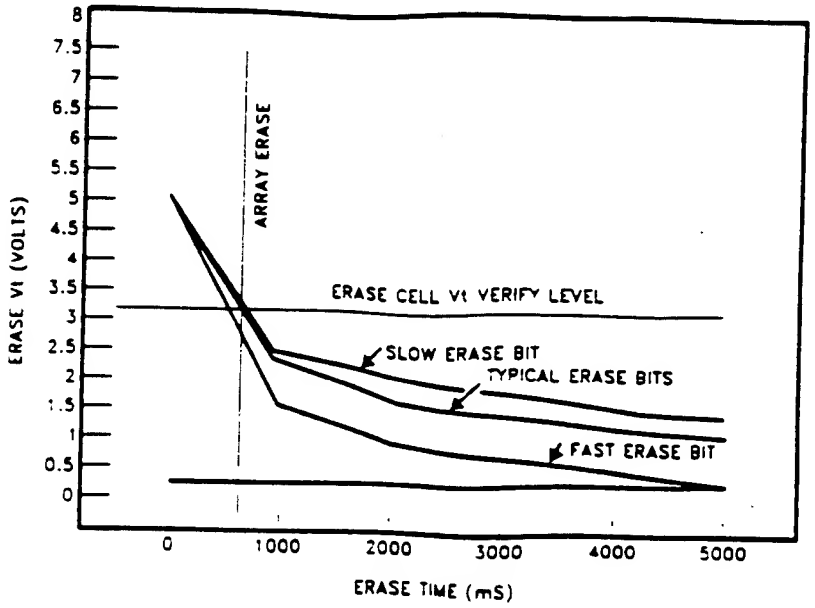

Figure 8. Array Erase Vt vs. Erase Time

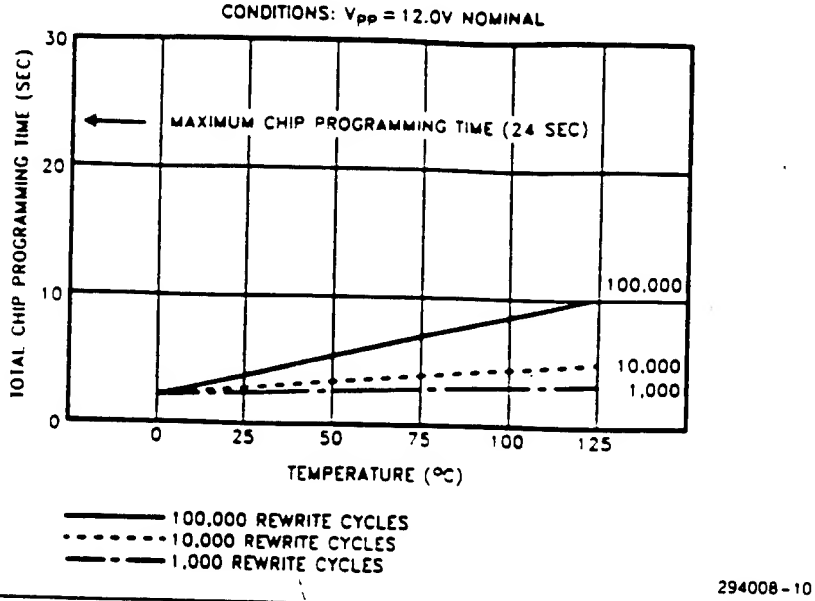

Figure 9. 28F010 Typical Programming Time vs. Temperature

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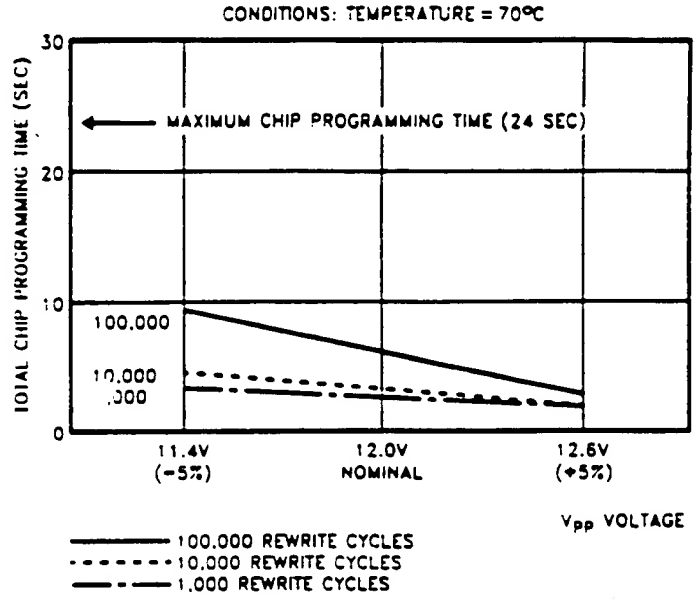

Figure 10. 28F010 Typical Programming Time vs. V_{PP} Voltage

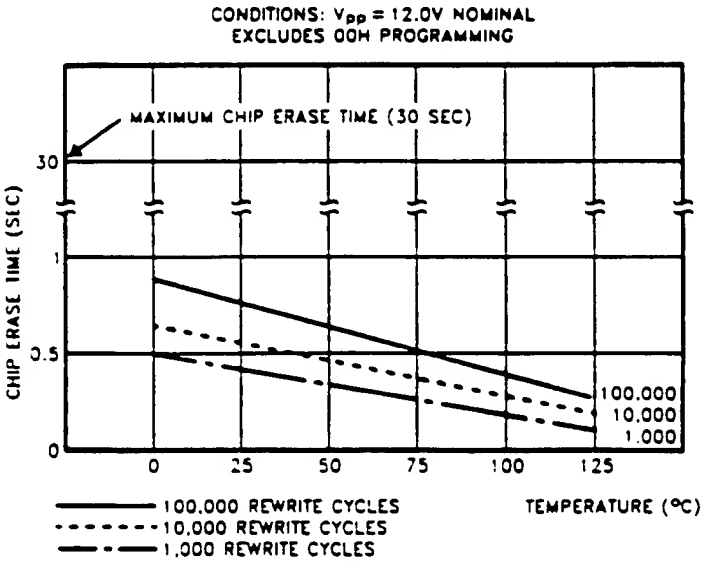

Figure 11. 28F010 Typical Erase Time vs. Temperature

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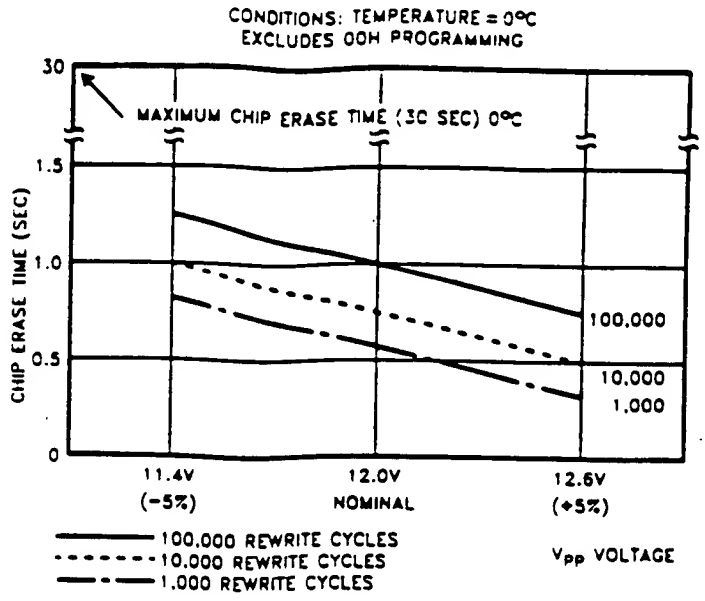

Figure 12. 28F010 Typical Erase Time vs. V_{PP} Voltage

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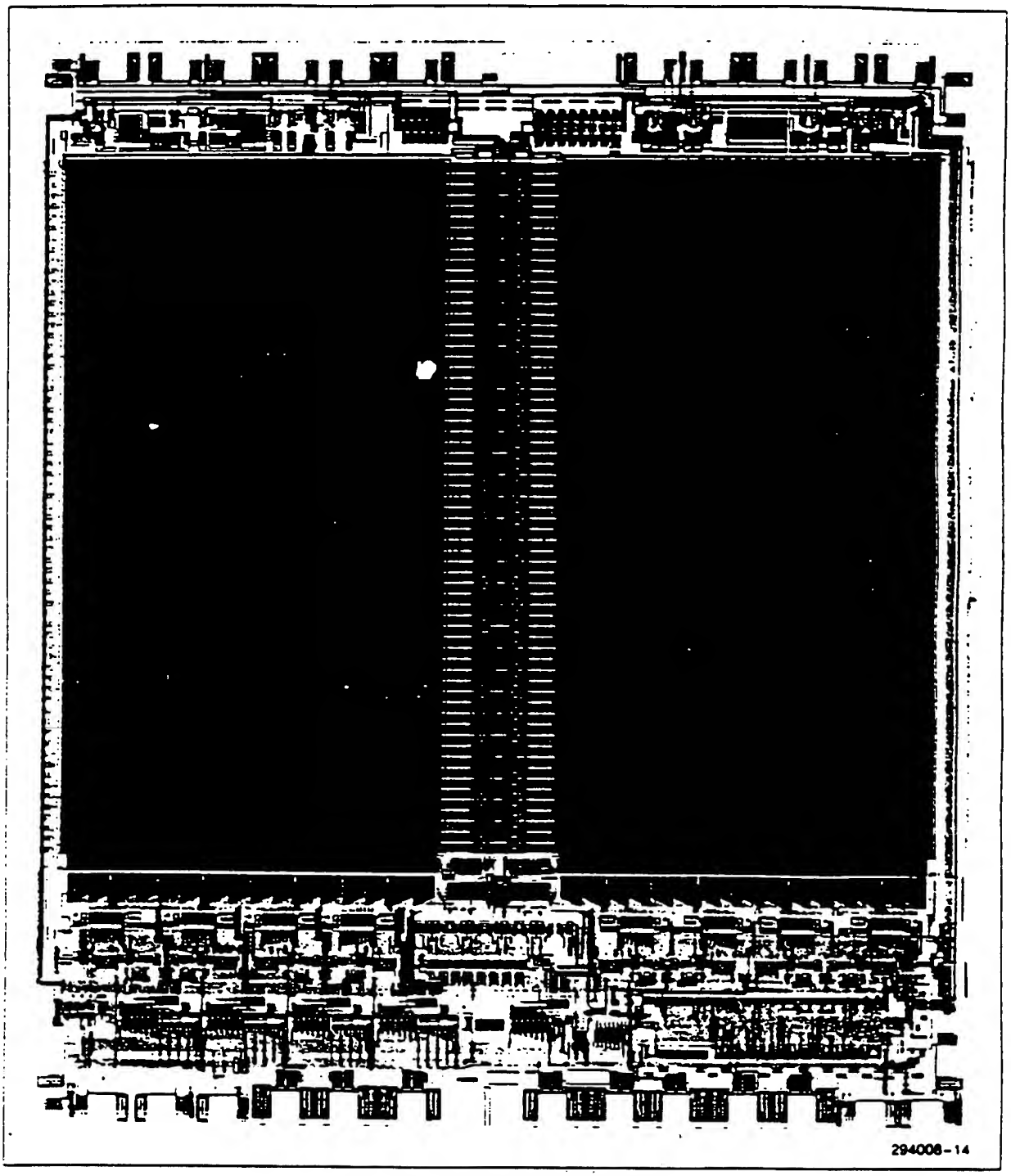

Figure 13. 28F010 Die Photograph

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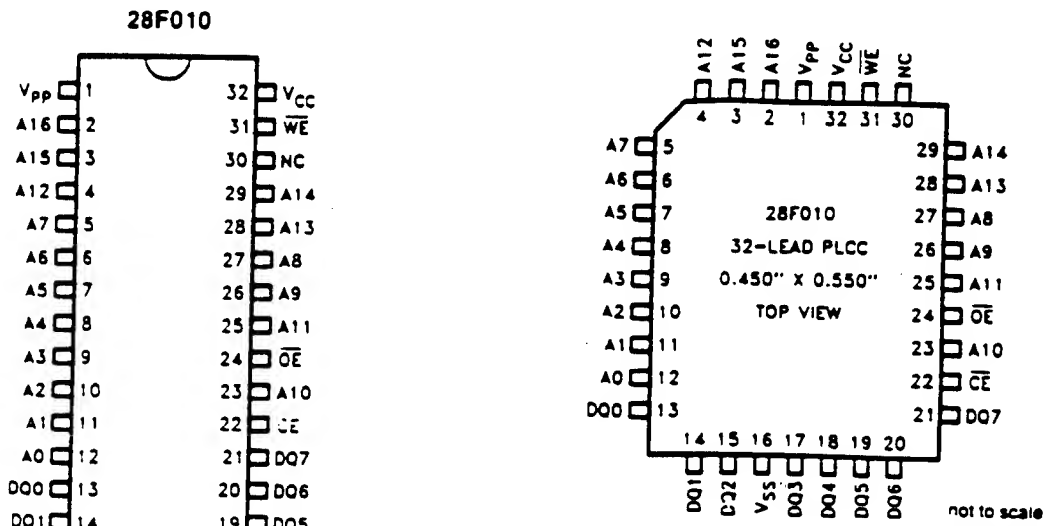

Pin Names

A_0–A_{16}	Address Inputs
DQ_0–DQ_7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{PP}	Program/Erase Power
V_{CC}	Device Power
V_{SS}	Ground

Figure 14. 28F010 Pin Configurations

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Columns are number 0 through 511 beginning with the column nearest the X-decoder.
Outputs are grouped as follows:

							Left Half Array O0 O1 O2 O3		Right Half Array O4 O5 O6 O7	
Address							Bitlines			
A16	A15	A10	A2	A1	A0	A3	IO0/7	IO1/6	IO2/5	IO3/4
0	0	0	0	0	0	0	BL384	BL256	BL128	BL0
0	0	0	0	0	0	1	BL385	BL257	BL129	BL1
0	0	0	0	0	1	0	BL386	BL258	BL130	BL2
0	0	0	0	0	1	1	BL387	BL259	BL131	BL3
0	0	0	0	1	0	0	BL388	BL260	BL132	BL4
0	0	0	0	1	0	1	BL389	BL261	BL133	BL5
0	0	0	0	1	1	0	BL390	BL262	BL134	BL6
0	0	0	0	1	1	1	BL391	BL263	BL135	BL7
•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	0	0	BL508	BL380	BL252	BL124
1	1	1	1	1	0	1	BL509	BL381	BL253	BL125
1	1	1	1	1	1	0	BL510	BL382	BL254	BL126
1	1	1	1	1	1	1	BL511	BL383	BL255	BL127

Figure 15. Bitline Decoding

X Address										Row
A14	A12	A7	A6	A5	A4	A13	A11	A9	A8	WL -
0	0	0	0	0	0	0	0	0	0	XL0
0	0	0	0	0	0	0	0	0	1	XL1
0	0	0	0	0	0	0	0	1	0	XL2
0	0	0	0	0	0	0	0	1	1	XL3
0	0	0	0	0	0	0	1	0	0	XL4
0	0	0	0	0	0	0	1	0	1	XL5
0	0	0	0	0	0	0	1	1	0	XL6
0	0	0	0	0	0	0	1	1	1	XL7
0	0	0	0	0	0	1	0	0	0	XL8
0	0	0	0	0	0	1	0	0	1	XL9
0	0	0	0	0	0	1	0	1	0	XL10
0	0	0	0	0	0	1	0	1	1	XL11
0	0	0	0	0	0	1	1	0	0	XL12
0	0	0	0	0	0	1	1	0	1	XL13
0	0	0	0	0	0	1	1	1	0	XL14
0	0	0	0	0	0	1	1	1	1	XL15
0	0	0	0	0	1	1	1	1	1	XL16
0	0	0	0	0	1	1	1	1	0	XL17
0	0	0	0	0	1	1	1	0	1	XL18
0	0	0	0	0	1	1	1	0	0	XL19
0	0	0	0	0	1	1	0	1	1	XL20
0	0	0	0	0	1	1	0	1	0	XL21
0	0	0	0	0	1	1	0	0	1	XL22
0	0	0	0	0	1	1	0	0	0	XL23
0	0	0	0	0	1	0	1	1	1	XL24
0	0	0	0	0	1	0	1	1	0	XL25
0	0	0	0	0	1	0	1	0	1	XL26
0	0	0	0	0	1	0	1	0	0	XL27
0	0	0	0	0	1	0	0	1	1	XL28
0	0	0	0	0	1	0	0	1	0	XL29
0	0	0	0	0	1	0	0	0	1	XL30
0	0	0	0	0	1	0	0	0	0	XL31

Figure 16. Wordline Decoding

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X Address										Row
A14	A12	A7	A6	A5	A4	A13	A11	A9	A8	WL
0	0	0	0	1	0	0	0	0	0	XL32
•	•	•	•	•	•	•	•	•	•	• • •
0	0	0	0	1	0	1	1	1	1	XL47
0	0	0	0	1	1	1	1	1	1	XL48
•	•	•	•	•	•	•	•	•	•	• • •
0	0	0	0	1	1	0	0	0	0	XL63
0	0	0	1	0	0	0	0	0	0	XL64
•	•	•	•	•	•	•	•	•	•	• • •
0	0	0	1	0	0	1	1	1	1	XL79
0	0	0	1	0	1	1	1	1	1	XL80
•	•	•	•	•	•	•	•	•	•	• • •
0	0	0	1	0	1	0	0	0	0	XL95
1	1	1	1	1	0	0	0	0	0	XL992
•	•	•	•	•	•	•	•	•	•	• • •
1	1	1	1	1	0	1	1	1	1	XL1007
1	1	1	1	1	1	1	1	1	1	XL1008
•	•	•	•	•	•	•	•	•	•	• • •
1	1	1	1	1	1	0	0	0	0	XL1023

Figure 16. Wordline Decoding (Continued)

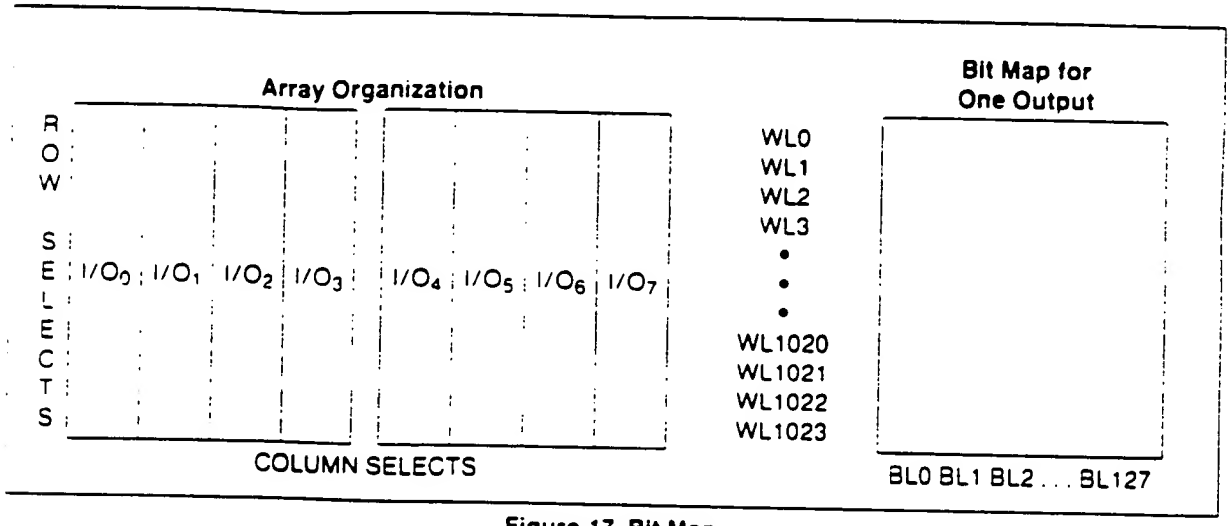

Figure 17. Bit Map

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intel®

RELIABILITY REPORT

RR-60

October 1989

ETOX™ Flash Memory Reliability Data Summary

SAN040130

Order Number: 293002-006

THE IMPORTANCE OF RELIABILITY

Reliability of the non-volatile memories in your end product is critical to your total system reliability. The use of Intel flash memories can make a difference. Reliability is not just tested, but designed into each component Intel manufactures.

Quality = Reliability

A quality component is one that meets your specification when received and tested. A reliable component continues to meet your specification even years after you have shipped your product.

CONSIDER QUALITY VS. RELIABILITY

The true cost of any component involves more than just the purchase price. The true component cost encompasses the initial purchase price, cost of rework during system production, and the cost of field repairs due to component failures. "Rework" costs during system production are incurred prior to shipment of your end product, and are a function of the quality of the component you purchase.

Repair costs incurred in the field after end product shipments, are a function of the reliability of the components. In addition to the increasing real cost of a system field service call, there is the intangible cost of a poor reliability reputation to the end use of your product. These costs depend upon the reliability of the components you purchase. Thus, reliability may impact costs during the system lifetime more than the initial quality of the components!

In-circuit reprogrammability of flash memories enables the addition of production line testing and system level screening. This capability, along with the inherent reliability of Intel flash components, provides your systems with significant reliability enhancements. Soldering the flash memory directly to the board enhances contact integrity. Since flash memories do not have to be removed for reprogramming, reliability risk due to handling is eliminated upon device installation. In addition, single socket testing reduces component handling during incoming inspection.

Monitor Program

Reliability is designed into each component Intel manufactures. From the moment the design is put to paper, stringent reliability standards must be met at each step for a product to bear the Intel name.

Designing-in reliability, however, is only the beginning. Ongoing tests must be conducted to ensure that the original reliability specifications remain as valid in volume production as they were when the device was first qualified.

Intel's Reliability Monitor Program, devised to measure and control device reliability in production, is available to our customers. The Monitor Program subjects all of Intel's technologies to a 48 hour dynamic burn-in at 125°C (with a portion of these devices continued for a 1000 hour lifetest) and provides answers about device reliability that are not generally available from limited testing programs. When test rejects are encountered, failure analysis is performed on each failed part. Isolating the fault and determining the failure mechanism is a critical part of the Monitor Program.

The primary objective is to deliver reliable, quality devices. Actions that Intel takes to meet this objective may include a process or design change, or added reliability screen. Each decision is made with our customers in mind so that they receive the parts—and the performance—that they ordered by specifying Intel. Reliability qualification assures that all new production material meets Intel's reliability standards. The Reliability Monitor Program ensures that these high standards are continually maintained over the duration of a device's life. This reliability improves the lifetime reputation of your product, reducing the required number of field service calls.

ETOX™ FLASH MEMORY TECHNOLOGY OVERVIEW

Intel's ETOX™ and ETOX II (EPROM tunnel oxide) flash memory technologies* consist of a non-volatile memory cell that electrically erases in bulk array form. Derived from Intel's CHMOS** II-E EPROM technology, ETOX flash memory technology combines the EPROM program mechanism with the E^2PROM erase mechanism. The memory cell is composed of a single transistor with a floating gate for charge storage, like the conventional EPROM. The primary difference between flash memory and EPROM cells is the flash memory cell's thinner gate oxide, which enables the electrical erase capability. This report compares and contrasts ETOX technology and EPROM reliability, describes Intel's flash reliability testing methodology, and summarizes the reliability data of Intel's flash memories.

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*Intel's ETOX flash memory process has patents pending.
**CHMOS is a patented process of Intel Corporation.

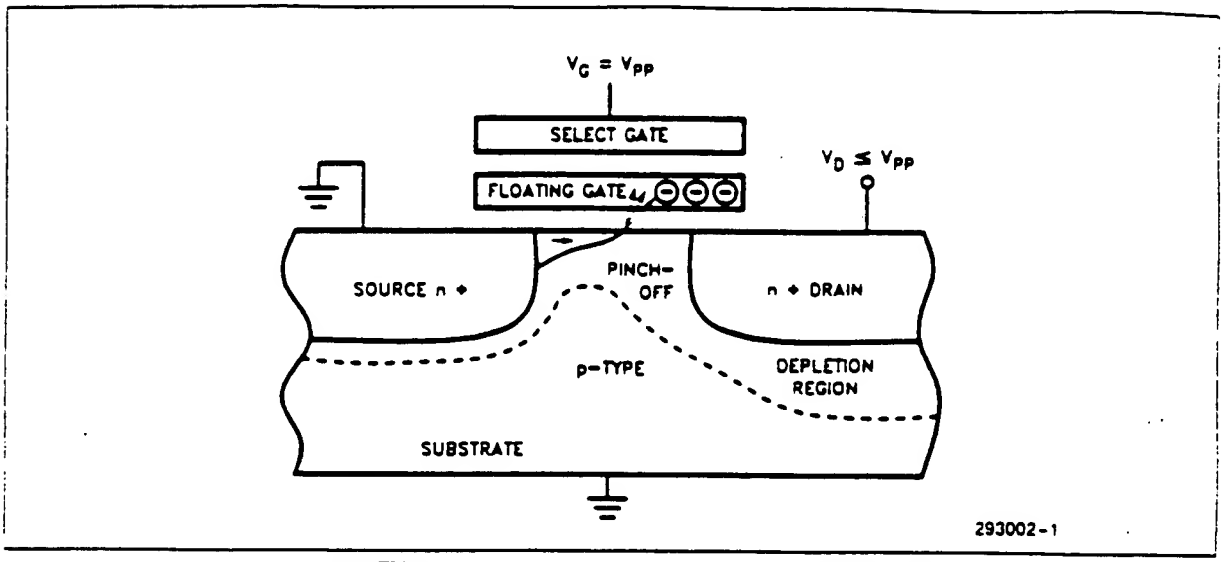

Figure 1. ETOX™ Flash Memory Cell during Programming (Side View)

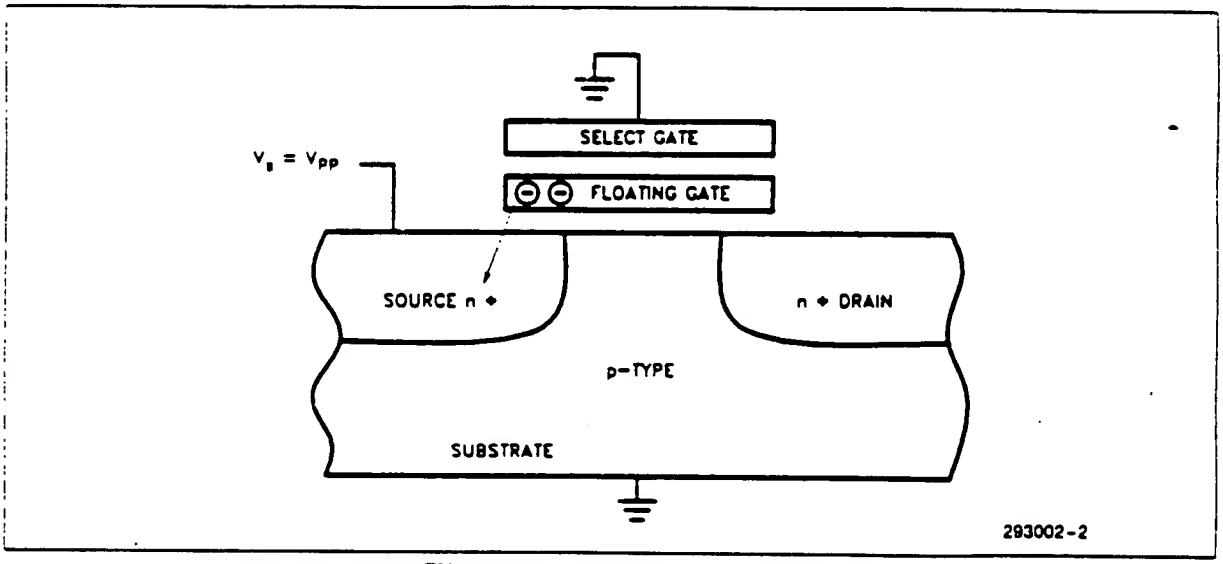

Figure 2. ETOX™ Flash Memory Cell during Erase (Side View)

Similarities with EPROM

When in program mode, a flash memory behaves exactly like a conventional EPROM. A high drain voltage generates "HOT" electrons that are swept across the channel. High voltage on the control gate attracts these free electrons across the lower gate oxide into the floating gate, where they are trapped. See Figure 1. Thus, ETOX flash memory cells exhibit the same reliability characteristics as conventional EPROMs during program mode even with a thinner oxide. When in read mode, a flash memory behaves just like an EPROM.

Differences from EPROM

With respect to functionality, the major difference between flash memory technology and EPROM technology lies with the erase mechanism. For EPROM cells, ultraviolet light neutralizes the charge on the floating gate, thus erasing the cell. For ETOX flash memory cells, an electric field across the lower gate oxide pulls electrons off the floating gate to the source region, thus erasing the cell. See Figure 2. This erase mechanism is an E^2PROM adaptation using "Fowler-Nordheim"(1) tunneling. The electric field during erase is the only new stress compared to EPROM that may impact overall reliability.

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Erase/Write Cycling

Failure mechanisms traditionally associated with cycling electrically erasable memories include charge loss due to defective bits, destructive oxide breakdown, and electron trapup. ETOX flash memory technology minimizes these failure mechanisms by improvements in process technology, reducing the electric field stressing the gate oxide, and using efficient erase/write algorithms to control programming and erasure.

OXIDE QUALITY

Thin oxides used in tunnelling have been a reliability concern for electrically erasable memories. The quality of the ETOX tunnel oxide is approximately 10 times better than that of other tunnel oxide approaches. This breakthrough in tunnel oxide quality results from explicit process improvements and through the implicit advantages of the ETOX flash cell approach.

OXIDE BREAKDOWN

Oxide breakdown, due to erase/write cycling, has also been a major reliability concern for thin oxide tunnelling. ETOX technology addresses this concern by reducing the amount of stress placed on the tunnel oxide during programming and erasure. First, erasing the flash cell involves tunnelling only through the gate/source overlap, thus reducing the area under stress. This, coupled with the improvement in oxide quality, lowers the probability of an oxide defect. Secondly, the flash cell is erased using a lower-voltage erase pulse, resulting in lower stress on the tunnel oxide. This lower electric field across the tunnel oxide (10MV/cm versus 12MV/cm) yields a theoretical wear out time 10^8 times longer than other E^2PROM approaches.

ELECTRON TRAPUP

The phenomenon of electron trapup, the gradual reduction of electron mobility through the tunnel oxide, results in increasing program and erase times as cycling occurs. The program and erase algorithms must apply more pulses to add charge to or bleed charge off the floating gate to ensure data retention and integrity. This is seen as a failure to program or erase within the algorithm's allowed time and not as a hard failure. The Quick-Pulse Programming™ and Quick-Erase™ algorithms maintain an efficient program and erase time for the specified number of cycles listed in the flash memory data sheets.

ETOX™ FLASH MEMORY RELIABILITY TESTING

Intel flash memories undergo comprehensive testing to insure electrical reliability. This testing is done at qualification and during ongoing monitor checks.

Information on flash memory reliability testing procedures follows.

High Temperature 5.25V Dynamic Lifetest—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test, the memory is sequentially addressed and the outputs are exercised, but not monitored or loaded. A checkerboard data pattern is used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with the failure analysis.

In order to best determine long-term failure rate, all devices used for lifetesting are subjected to standard INTEL testing. The 48 hour burn-in results are an indication of infant mortality and are not included in the failure rate calculation. (See Figure 3 for typical burn-in bias and timing diagrams.)

High Temperature High Voltage Dynamic Lifetest—This test is used to accelerate oxide breakdown failures. The test setup is identical to the one used for the dynamic lifetest except V_{CC} is increased. The acceleration factor due to this test can be found in Table 2. This data plus the standard dynamic lifetest data are used to calculate the 0.3 eV failure rate (See Figure 4 for typical bias and timing diagram).

Data Retention Bake—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 98% programmed pattern to a 250°C bake with no applied bias. In addition to data retention, this test is used to detect mechanical reliability problems (e.g., bond integrity) and process instability.

Temperature Cycle—This test consists of cycling the temperature of the chamber housing the subject devices from −65°C to +150°C and back. One thousand cycles are performed with a complete cycle taking 20 minutes. This test is to detect mechanical reliability problems and microcracks.

Low Temperature Lifetest—This test is performed at −10°C to detect the effects of hot electron injection into the gate oxide as well as package related failures (e.g., metal corrosion, etc.).[4]

SAN040133

ESD Testing—This test is performed to validate the product's tolerance to Electro Static Discharge damage. All products incorporate ESD protection networks on appropriate pins.

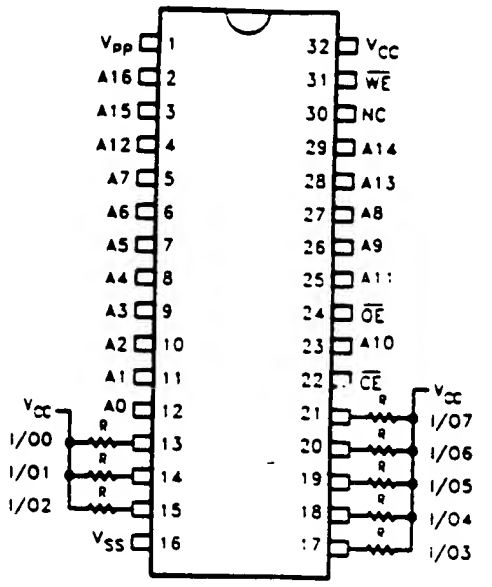
Two types of tests are performed. First, all devices are tested using Mil STD 883 test criteria. In addition, a charged device test is performed to further validate protection occurring during mechanical handling.

Erase/Write Cycling (ETOX™ Flash Memories)—This test consists of repeatedly programming the device to an all 00H pattern and then erasing to all 0FFH data. Worst case voltage levels are used to maximize charge transfer to and from the floating gates. Cycling is used to ensure devices meet reprogrammability requirements as well as precondition for other reliability stresses.

Failure Rate Calculations

Failure rate calculations are given for each relevant activation energy. Failure rate calculations are made using the appropriate energy [2,3,4,5] and the Arrhenius Plot as shown in Figure 5*. The total equivalent device hours at a given temperature can be determined. The failure rate is then calculated by dividing the number of failures by the equivalent device hours and is expressed as a %/1000 hours. To arrive at a confidence level associated failure rate, the failure rate is adjusted by a factor related to the number of device hours using a chi-square distribution. A conservative estimate of the failure rate is obtained by including zero failures at 0.3 eV. Devices submitted to stresses other than lifetest received a 168 hour lifetest prior to stressing.

*NOTE:
The activation energies for various failure mechanisms are listed in Table 1. The methodology for calculating failure rates is detailed in Appendix A.



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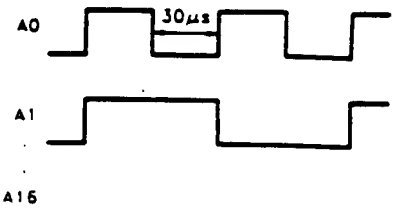
$\overline{OE}$ = −5.25V, R = 1 kΩ, V_{CC} = −5.25V.
$\overline{PGM}$ = −5.25V
V_{PP} = 5.25V.
V_{SS} = GND, $\overline{CE}$ = GND



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Binary Sequence from A_0 to A_{16}

Figure 3. 28F010 Burn-In Bias and Timing Diagrams

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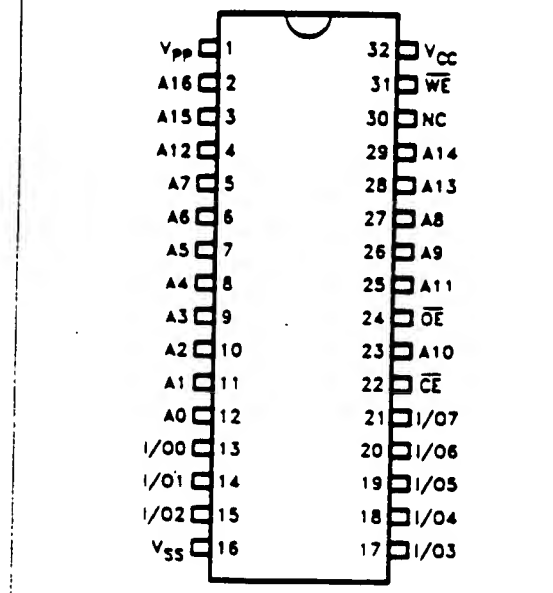

Figure 4. 28F010 Lifetest Bias and Timing Diagram

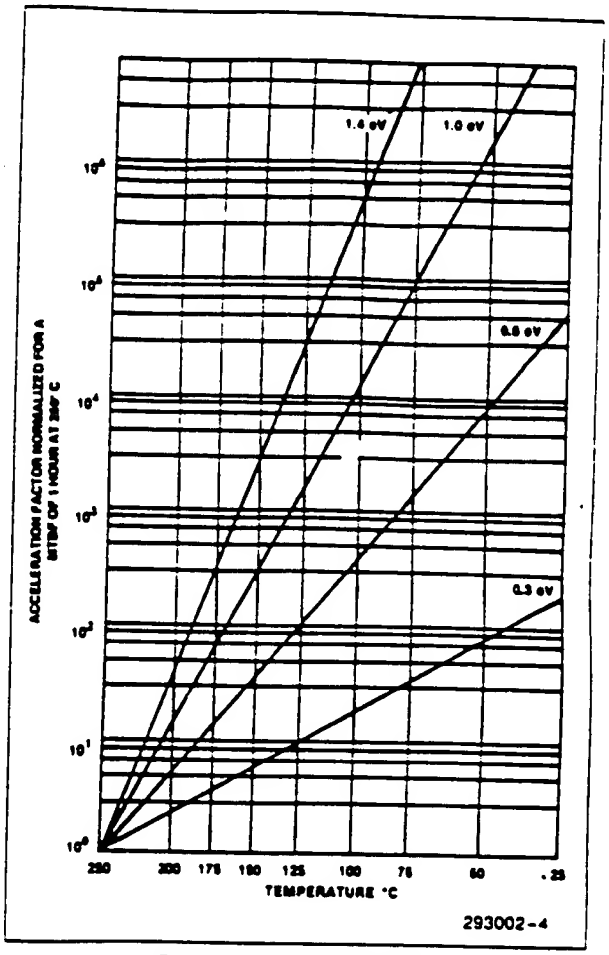

Figure 5. Arrhenius Plot

Table 1. Failure Mechanism Activation Energies Relevant to ETOX Flash Memories

Failure Mode	eV
Oxide	0.3
SBCL/SBCG/MBCL/MBCG	0.6
Contamination	1.0
Speed Degradation	0.3-1.0
Intrinsic Charge Loss	1.4
Contact Spiking	0.8

A typical lifetest bias and timing diagram is shown in Figure 4.

SAN040135

Type	Supply Voltage (Volts)	Oxide Thickness (Å)	Operating Stress (MV/CM)	Acceleration Factor at __% Over Stress				
				10%	20%	30%	50%	100%
CHMOS IIE	5	400	1.25	7.5	55	422	3162	5.6E−5
CHMOS III E	5	235	2.13	3.7	13.4	49.1	658	4.3E−5
ETOX™	5	400	1.25	7.5	55	422	3162	5.6E−8
ETOX II	5	235	2.13	3.7	13.4	49.1	658	4.3E−5

ASSUMES:
1. No bias generators
2. Depletion loads
3. Failure rate calculations use the appropriate acceleration factor for stress voltage and maximum operating voltage (conservative).
4. See reference 7 for VAF determination.

Table 2. Time-Dependent Oxide Failure Acceleration

RELIABILITY DATA SUMMARY

The following data is an accumulation of recent qualification and monitor program results. Failure rate calculation methods listed in Appendix A were used to arrive at the tabularized failure rates.

In reviewing the reliability data as presented, questions may arise as to why lot sizes often decrease from one test to another without a corresponding number of identified failures. This is due to a variety of factors. Many tests require smaller sample sizes and as a result all parts from a previous test do not necessarily flow through to a succeeding test.

In addition, various parts are pulled from a sample lot when mechanical or handler failures occur. These "failures" are not a result of the specific test just completed but are nonetheless removed from the sample lot size and are not included in any failure rate calculation. It can also happen that a particular test is done incorrectly through human error or faulty test equipment and "invalid" failures are put aside for retesting at a later date, decreasing the lot size for a succeeding test. If these parts are found to be truly defective, they are treated as failures and listed. If they test out properly, they are removed from any calculation data base.

References

1. M. Lenzlinger.E. H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2", Journal of Applied Physics, Vol. 40 (1969), p. 278.
2. S. Rosenberg, D. Crook, B. Euzent, "16th Annual Proceedings of the International Reliability Physics Symposium", pp. 19–25, 1978.
3. S. Rosenberg, B. Euzent, "HMOS Reliability" Reliability Report RR-18, Intel Corporation, 1979.
4. R. M. Alexander, "Calculating Failure Rates from Stress Data, April 1984 International Reliability Physics Symposium.
5. "EPROM Reliability DATA Summary" Reliability Report RR-35, Intel Corporation, 1985.
6. "E^2PROM and NVRAM Reliability DATA Summary" Reliability Report RR-59B, Intel Corporation, 1986.
7. E.S. Anolick, G.R. Nelson, "Low Field Time Dependent Dielectric Integrity", 1979 International Reliability Physics Symposium, pp. 8–12.

NOTE:
The methodology for calculating failure rates is detailed in Appendix A.

SAN040136

27F64

The Intel 27F64 (CERDIP) is a 64K Electrically Bulk-Erasable Flash Memory.

Number of Bits:	65,536
Organization:	8,192 × 8
Pin Out:	28-pin CERDIP
Die Size:	115 × 132 mils
Process:	ETOX™ Flash Memory
Cell Size:	6.0 × 6.0 μM
Programming Voltage:	12.75 VOLTS EXTERNAL
Technology:	CMOS

Table 1. Reliability Data Summary

Year	Burn-In	125°C Dynamic Lifetest			7.0V Dynamic Lifetest				
	48 Hours	168 Hrs	500 Hrs	1K Hours	2K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1988	0/3615	1/3602	1/992	0/990	0/990	0/432	0/432	0/432	0/432
Total	0/3615	1/3602	1/992	0/990	0/990	0/432	0/432	0/432	0/432
		A	A						

Table 2. Additional Qualification Tests

Year	Program/Erase Cycling		250°C Data Retention Bake					
			48 Hours		168 Hours		500 Hours	
	100	20K	Noncycled	Cycled	Noncycled	Cycled	Noncycled	Cycled
1988	0/1396	0/100	0/125	0/390	0/125	2/390	1/125	1/388
Total	0/1396	0/100	0/125	0/390	0/125	2/390	1/125	1/388
						A	A	A

Failure Analysis: A—Single bit charge loss

Table 3. 27F64 Failure Rate Prediction

125°C Actual Device Hours	Ea eV	Equivalent Hours		# Fail	Failure Rate %/1K Hours (60% U.C.L.)	
		55°C	70°C		55°C	70°C
2.25E − 06	0.3 BI − ELT	1.33E − 07	8.40E − 06	0	—	—
4.32E − 05	0.3 HVELT VAF*	1.08E − 09	6.80E − 08	0	0.00008	0.00013
2.69E − 06	0.6 BI − ELT − HVELT	9.20E − 07	3.60E − 07	2	0.0045	0.0110
2.69E − 06	1.0 BI − ELT − HVELT	9.60E − 08	2.00E − 07	0	0.0009	0.0046
			Combined Failure Rate:		0.0054	0.0157
			FITs:		54	157

*VAF (Voltage Acceleration Factor) for HVELT = 422

NOTE:
125°C Dynamic Lifetest and 7.0V Dynamic Lifetest samples each contain a split between units which saw 100 p/e cycles before stress and those which did not.

SAN040137

28F256

The Intel 28F256 is a 256-kilobit bulk-erasable flash memory.

Number of Bits:	262,144	Process:	ETOX™ Flash Memory
Organization:	32,768 × 8	Technology:	CMOS
Pin Out:	32-pin CERDIP	Cell Size:	6.0 × 6.0 μM
Die Size:	181 × 203 mils	Programming Voltage Options:	(P1) 12.0V +/−5%

Table 1. Reliability Data Summary

Year	Burn-In	125°C Dynamic Lifetest				7.25V Dynamic Lifetest				
	48 Hours	168 Hrs	500 Hrs	1K Hours	2K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1988	1/17622	1/17620	1/945	0/941	0/430	0/458	0/456	0/456	0/152	0/95
1989	0/5428	0/5426	0/432	0/432	0/332	0/466	0/466	0/215	0/215	—
Total	1/23050	1/23046	1/1377	0/1373	0/752	0/924	0/922	0/671	0/367	0/95
	A	B	C							

Table 2. Additional Qualification Tests

Year	Program/Erase Cycling	250°C Data Retention Bake					
		48 Hours		168 Hours		500 Hours	
	100	Noncycled	Cycled	Noncycled	Cycled	Noncycled	Cycled
1988	0/1867	0/735	1/437	0/733	2/436	1/585	3/143
1989	0/800	0/900	0/500	1/874	0/500	5/873	1/497
Total	0/2667	0/1635	1/937	1/1607	3/936	6/1458	4/640
			D	D	D	D	E

Year	Temperature Cycling			Thermal Shock		
	200 Cycles	500 Cycles	1K Cycles	50 Cycles	200 Cycles	500 Cycles
1988	0/233	0/223	0/223	0/224	0/224	0/224
1989	0/175	0/175	0/175	0/125	0/125	0/125
Total	0/398	0/398	0/398	0/349	0/349	0/349

NOTE:
The 250°C Data Retention Bake samples labeled "Noncycled" received no program/erase cycling prior to Bake. "Cycled" units first saw 100 p/e cycles.

SAN040138

28F256 Failure Rate Prediction

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hours	
		55°C	70°C		55°C	70°C
4.66×10^6	0.3 BI	2.74×10^7	1.78×10^7	0		
6.56×10^5	0.3 × VAF	2.12×10^8	1.38×10^8	0		
		TOTAL 0.3 eV Failures =		0	0.0001	0.0001
4.66×10^6	0.6 BI	1.62×10^8	6.81×10^7	2		
6.56×10^5	0.6 HVELT	2.27×10^7	9.58×10^6	0		
		TOTAL 0.6 eV Failures =		2	0.0017	0.0040
4.66×10^6	1.0 BI	1.72×10^9	4.07×10^8	0		
6.56×10^5	1.0 HVELT	2.42×10^8	5.73×10^7	0		
		TOTAL 1.0 eV Failures =		0	0.0000	0.0002
			Combined Failure Rate:		0.0018	0.0043
			FITs:		18	43

θ_{JA} = 79°C/W
V_{CC} = 5.25V
I_{CC} @55 = 18 mA
I_{CC} @70 = 17 mA
I_{CC} @125 = 16 mA

Temp with θ_{JA}
T(55) = 335.6K
T(70) = 350.2K
T(125) = 404.7K
T(250) = 523.1K

k = 8.62E−05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3	5.886	3.821
Accel.	0.6	34.65	14.60
Factors:	1.0	368.3	87.24

Voltage Accel. Factor (VAF)
for HVELT on this process is = 422.0

Failure Analysis:
A. 1-Single bit charge gain (pass. defect)
B. 1-Single bit charge gain (metal defect)
C. 1-Multiple bit charge loss (pass. defect)
D. 1-Single bit charge loss
E. 3-Single bit charge loss
1-Open bond wire

SAN040139

28F512

The Intel 28F512 is a 512-Kbit bulk-erasable flash memory.

Number of Bits:	524,288	Process:	ETOX II Flash Memory
Organization:	65,536 × 8	Technology:	CMOS
Pin Out:	32-pin CERDIP/PLCC	Cell Size:	3.8 × 4.0 μM
Die Size:	227 × 181 mils	Programming Voltage Options:	12.0V ±5%

Table 1. Reliability Data Summary

Year	Burn-In	125°C Dynamic Lifetest			7.0V Dynamic Lifetest			
	48 Hours	168 Hrs	500 Hrs	1K Hours	48 Hrs	168 Hrs	500 Hrs	1K Hrs
1989	0/100	1/100	0/99	1/99	0/300	0/299	0/298	1/220
Total	0/100	1/100	0/99	1/99	0/300	0/299	1/298	1/220
		A		B			C	D

Table 2. Additional Qualification Tests

Year	Program/Erase Cycling	250°C Data Retention Bake					
		48 Hours		168 Hours		500 Hours	
	10K	Noncycled	Cycled	Noncycled	Cycled	Noncycled	Cycled
1989	2/706	1/63	0/62	0/62	0/62	0/62	0/62
Total	2/706	1/63	0/62	0/62	0/62	0/62	0/62
	D	E					

Year	Temperature Cycling			Thermal Shock		
	200 Cycles	500 Cycles	1K Cycles	50 Cycles	200 Cycles	500 Cycles
1989	0/80	0/80	0/80	0/79	0/79	0/79
Total	0/80	0/80	0/80	0/79	0/79	0/79

NOTE:
250°C Data Retention Bake "Cycled" units received 10,000 program/erase cycles prior to Bake. 125°C Dynamic Lifetest and 7.0V Dynamic Lifetest samples contain a mix of cycled and uncycled material.

SAN040140

28F512 Failure Rate Prediction

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hours	
		55°C	70°C		55°C	70°C
9.44×10^4	0.3 BI	5.65×10^5	3.68×10^5	0		
2.59×10^5	0.3 × VAF	1.43×10^8	9.46×10^7	0		
		TOTAL 0.3 eV Failures =		0	0.0006	0.0010
9.44×10^4	0.6 BI	3.39×10^6	1.42×10^6	1		
2.59×10^5	0.6 HVELT	9.29×10^6	3.91×10^6	0		
		TOTAL 0.6 eV Failures =		1	0.0159	0.0386
9.44×10^4	0.8 BI	1.12×10^7	3.52×10^6	0		
2.59×10^5	0.8 HVELT	3.07×10^7	9.66×10^6	2		
		TOTAL 0.8 eV Failures =		2	0.0074	0.0242
9.44×10^4	1.0 BI	3.68×10^7	8.71×10^6	1		
2.59×10^5	1.0 HVELT	1.01×10^8	2.39×10^7	0		
		TOTAL 1.0 eV Failures =		1	0.0015	0.0060
			Combined Failure Rate:		0.0254	0.0702
			FITs:		254	702

θ_{JA} = 59°C/W
V_{CC} = 5.25V
I_{CC} @55 = 13 mA
I_{CC} @70 = 12 mA
I_{CC} @125 = 8 mA

Temp with θ_{JA}
T(55) = 332.1K
T(70) = 346.8K
T(125) = 400.6K
T(250) = 523.1K

k = 8.62E−05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3		3.845
Accel.	0.6	35.93	14.87
	0.8	118.6	36.29
Factors:	1.0	391.2	89.09

Voltage Accel. Factor (VAF)
for HVELT on this process is = 93.3

A. Multiple bit charge loss (contamination)
B. Single bit charge loss
C. 1-V_{MIN} due to single leaky col
D. 1-Basic function due to single leaky col
E. 1-Adjacent column failure due to metal stringer
   1 = ISB Failure Analysis pending assumed valid
F. 1-Multiple bit charge loss

SAN040141

28F010

The Intel 28F010 is a 1024-Kbit bulk-erasable flash memory.

Number of Bits:	1,048,576	Process:	ETOX™ II Flash Memory
Organization:	2 (512 × 1024)	Technology:	CMOS
Pin Out:	32-pin CERDIP	Cell Size:	3.8 × 4.0 μM
Die Size:	225 × 265 mils	Programming Voltage	12.0V ±5%

Table 1. Reliability Data Summary

Year	Burn-In	125°C Dynamic Lifetest				7.0V Dynamic Lifetest				
	48 Hours	168 Hrs	500 Hrs	1K Hours	2K Hrs	48 Hrs	168 Hrs	500 Hrs	1K Hrs	2K Hrs
1989	0/530	0/500	1/500	1/499	1/98	0/698	1/697	1/697	2/695	1/96
Total	0/530	0/500	1/500	1/499	1/98	0/698	1/697	1/697	2/695	1/96
			A	B	A		B	B	C	B

Table 2. Additional Qualification Tests

Year	Program/Erase Cycling		250°C Data Retention Bake					
			48 Hours		168 Hours		500 Hours	
	10K	100K	Noncycled	Cycled	Noncycled	Cycled	Noncycled	Cycled
1989	13/2169	3/48	0/306	0/307	0/306	0/307	0/85	0/120
Total	13/2169	3/48	0/306	0/307	0/306	0/307	0/85	0/120
	D	E						

Year	Temperature Cycling			Thermal Shock		
	200 Cycles	500 Cycles	1K Cycles	50 Cycles	200 Cycles	500 Cycles
1989	0/369	0/369	0/369	0/318	0/318	0/318
Total	0/369	0/369	0/369	0/318	0/318	0/318

NOTE:
250°C Data Retention Bake "Cycled" units received 10,000 program/erase cycles prior to Bake. 125°C Dynamic Lifetest and 7.0V Dynamic Lifetest samples contain a mix of cycled and uncycled material.

SAN040142

28F010 Failure Rate Prediction

125°C Actual Device Hours	Ea (eV)	Equivalent Hours		# Fail	Fail Rate %/1K Hours	
		55°C	70°C		55°C	70°C
5.735×10^5	0.3 BI	3.52×10^6	2.24×10^6	0		
7.920×10^5	0.3 × VAF	4.56×10^8	2.91×10^8	1		
			TOTAL 0.3 eV Failures =	1	0.0004	0.0007
5.735×10^5	0.6 BI	2.16×10^7	8.77×10^6	1		
7.920×10^5	0.6 HVELT	2.98×10^7	1.21×10^7	3		
			TOTAL 0.6 eV Failures =	4	0.0103	0.0248
5.735×10^5	0.8 BI			2		
7.920×10^5	0.8 HVELT			1		
			TOTAL 0.8 eV Failures =	3	0.0025	0.0080
			Combined Failure Rate:		0.0132	0.0335
			FITs:		132	335

θ_{JA} = 46°C/W
V_{CC} = 5.25V
I_{CC} @55 = 15 mA
I_{CC} @70 = 13 mA
I_{CC} @125 = 11 mA

Temp with θ_{JA}
T(55) = 331.7K
T(70) = 346.2K
T(125) = 400.8K
T(250) = 523.1K

k = 8.62E−05 eV/K

		Thermal Accel. Factors 55°C	70°C
BI/ELT	0.3	6.095	3.925
Accel.	0.6	37.14	15.41
	0.8	123.9	38.35
Factors:	1.0	413.5	95.42

Voltage Accel. Factor (VAF)
for HVELT on this process is = 93.3

A. Speed degrade (spiked contact)
B. Single bit charge loss
C. 1-Column failure (spiked contact)
   1-Speed degrade (analysis pending; 0.3 eV)
D. 7-Dual column (spiked contact)
   3-Column failure (spiked contact)
   2-Isb (analysis pending)
   1-Adjacent row (analysis pending)

E. 2-Single bit programming push-out
   1-Single bit failure (oxide defect)*

*NOTE:
Current production testing guarantees programming push-out screens for 10K cycles. 100K cycle screens are currently under development.

SAN040143

Plastic Reliability Data Summary

INTRODUCTION

The following information is written to provide users with the description and reliability summary of Intel's plastic flash product PLCC packages. It includes brief test descriptions, a description of plastic packaging compounds and the reliability data obtained during the qualification and subsequent product monitors of the N28F256. Qualification results for the N28F512 and N28F010 will be available in Dec 89.

PLASTIC PACKAGE CHARACTERISTICS

The plastic package is composed of flame retardant plastic/epoxy which meets the rating requirements of US94V0 1/8" minimum. The die attach incorporates a silver-filled adhesive die attach on a silver spot plated leadframe. Bonding is accomplished through gold thermal compression bonding and lead finish is either tin plated or 60/40 solder dipped tin/lead.

ELECTRICAL CHARACTERISTICS

Because of the electrical erase capabilities of Flash memories, parts may be programmed, 100% tested and erased in plastic packages.

Flash memories in plastic are tested to the same electrical/parametric levels as their counterparts in CERDIP. The characteristics include input/output voltage levels, speeds, leakage, and power requirement characteristics over the full commercial temperature operating range of 0°C–70°C. Performance capabilities are identical to that of CERDIP product.

RELIABILITY/QUALITY STRESSES

High Temperature 5.25V 125°C Dynamic Lifetest (HTDL)—This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. During the test, the memory is sequentially addressed and outputs are exercised but not monitored or loaded. A checkerboard data pattern is typically used to simulate random patterns expected during actual use. Results of lifetesting have been summarized along with failure analysis. In order to best determine long-term failure rates, all devices used for lifetesting are subjected to a standard Intel screening. The 48-hour burn-in results measure infant mortality and are not included in the failure rate calculations.

High Temperature Extended Lifetest (HTELT)—This test is also performed at 125°C but uses a smaller sample size. The parts are kept in the full active mode for the duration of the test with outputs driven. The test is intended to evaluate the long-term reliability of the product.

High Voltage Extended Lifetest (HVELT)—This test is used to accelerate oxide breakdown failures. The test is set up identical to the one used for dynamic lifetest except for V_{CC} and V_{PP} which are raised to 6.5V. The voltage acceleration factor for this configuration can be found in Table II.

Data Retention Bake—This test is used to accelerate charge loss from the floating gate. The test is performed by subjecting devices containing a 98% + program pattern to a 140°C bake with no applied bias. In addition to data retention, this test can also be used to detect mechanical reliability problems such as bond integrity or process instabilities.

85/85 TEST

During the 85°C/85% relative humidity test, the devices are subjected to a high temperature, high humidity environment. The object of the test is to accelerate failure mechanisms through an electrolytic process. This is accomplished through a combination of moisture penetration of the plastic, voltage potentials and contamination which, if present, would combine with the moisture to act as an electrolyte. See Figure 6 for typical 85/85 Bias Diagram.

Steam

SAN040144

Steam stressing performed at 121°C, 2 atm, accelerates moisture penetration through the plastic package material to the surface of the die. The objective of this test is to accelerate failures of the device as a result of moisture on the die surface. Corrosion, as typically seen in plastic encapsulated devices, is a very minor contributor to the Flash failure mechanisms. Due to the floating gate storage cell composition, Flash memories have a distinctive failure mode which requires special considerations and solutions.

The floating gate itself is a highly phosphorous doped structure on which electrons are stored, thus creating the non-volatile memory cell. Passivation defects or marginalities can allow moisture penetration to a single Flash cell causing oxide deterioration, thus showing up as a charge loss failure. This becomes the predominant failure mode for Flash product, opposed to corrosion which historically has been the dominant plastic mode of failure. Intel has developed a proprietary, multi-layer passivation which has successfully solved this problem.

QUALITY/RELIABILITY STANDARDS

The table below contains Intel's current requirements for qualification for plastic Flash memories. The failure rate criteria has been established based on a survey of major customers world-wide. Intel consistently meets or exceeds these requirements.

HTDL 48-Hr	HTELT 168/500-Hr	140°C Bake 48/168/500-Hr	HVELT 48/168-Hr	Steam 96/168-Hr	85/85 500/1K
<.05%	<200 FITs Combined Failure Rate			<2%/<5%	<1% Cum.

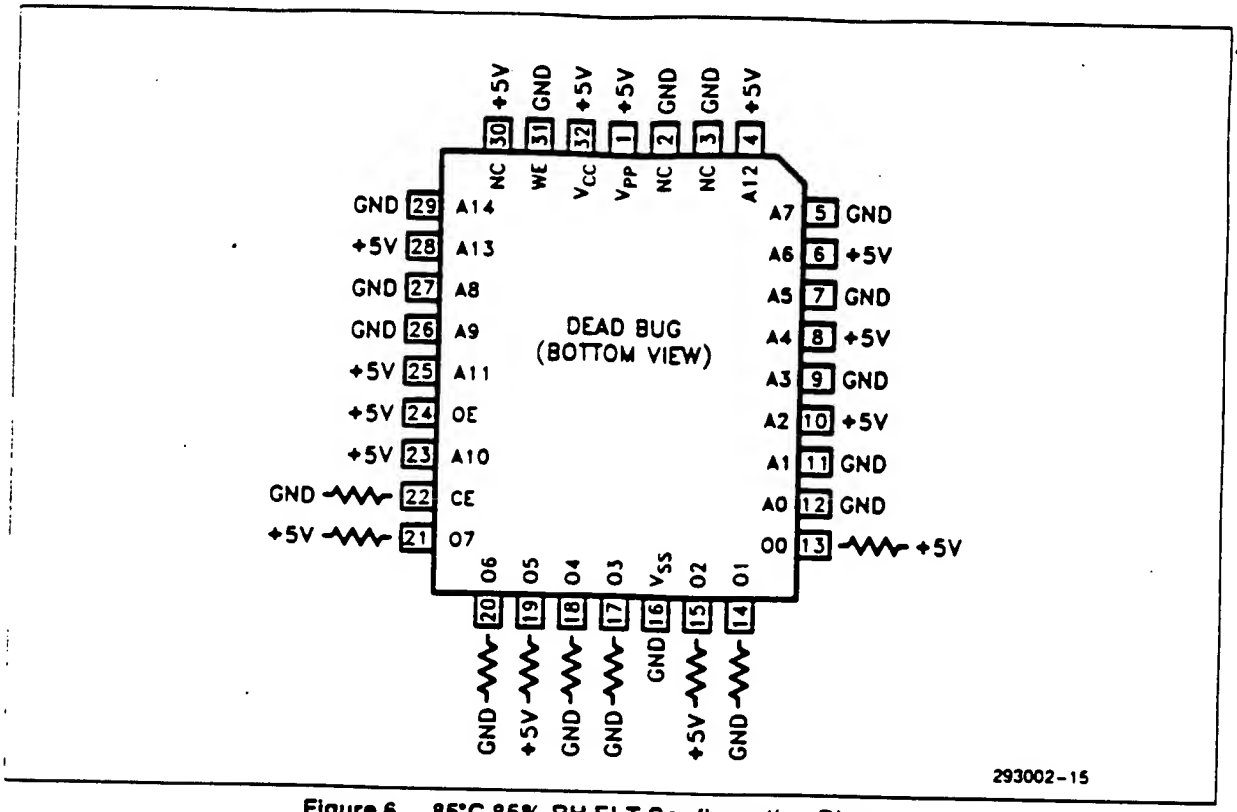

Figure 6. 85°C 85% RH ELT Configuration Diagram

SAN040145

N28F256

...cs are functionally identical to the D28F256 except that they are housed in a PLCC (N)

Table 1. Reliability Data Summary

	Burn-In	125°C Dynamic Lifetest				7.0V Dynamic Lifetest		
	48 Hours	168 Hrs	500 Hrs	1K Hours	2K Hrs	48 Hrs	168 Hrs	500 Hrs
1988	0/125	0/125	0/125	0/125	0/125	0/100	0/100	0/100
1989	—	—	—	—	—	—	—	—
Total	0/125	0/125	0/125	0/125	0/125	0/100	0/100	0/100

Table 2. Additional Qualification Tests

Year	140°C Data Retention Bake		
	48 Hours	168 Hours	500 Hours
1988	0/100	0/100	0/100
1989	—	—	—
Total	0/100	0/100	0/100

Year	Temperature Cycling			Thermal Shock		
	200 Cycles	500 Cycles	1K Cycles	50 Cycles	200 Cycles	500 Cycles
1988	0/50	0/50	0/50	0/50	0/50	0/50
1989	0/124	0/100	0/98	0/124	0/124	0/124
Total	0/174	0/150	0/148	0/174	0/174	0/174

Year	85°C/85% RH				Steam	
	168 Hrs	500 Hrs	1K Hrs	2K Hrs	168 Hrs	336 Hrs
1988	0/200	0/200	0/200	0/200	1/200	0/197
1989	0/497	0/497	0/497	0/371	0/497	0/493
Total	0/697	0/697	0/697	0/571	1/697	0/690
					A	

NOTE:
PLCC Monitor program is designed to monitor process/package environmental performance. Monitoring of electrical performance is accomplished via CERDIP 28F256 monitors.

SAN040146

N28F256 Failure Rate Prediction

125°C Actual Device Hours	Activation Energy (eV)	Equivalent Hours		# Fail	Failure Rate %/1K Hours (60% U.C.L.)	
		55°C	70°C		55°C	70°C
2.50E + 05	0.3 eV ELT	1.62E + 06	1.02E + 06	0		
5.00E + 04	0.3 eV HVLT × VAF	1.78E + 07	1.12E + 07	0		
	TOTAL 0.3 eV	1.94E + 07	1.22E + 07	0	0.00472	0.00750
2.50E + 05	0.6 eV ELT	1.05E + 07	4.13E + 06	0		
5.00E + 04	0.6 eV HVLT	2.09E + 06	8.27E + 05	0		
	TOTAL 0.6 eV	1.25E + 07	4.96E + 06	0	0.00729	0.01845
2.50E + 05	1.0 eV ELT	1.26E + 08	2.68E + 07	0		
5 0E + 04	1.0 eV HVLT	2.52E + 07	5.36E + 06	0		
	TOTAL 1.0 eV	1.51E + 08	3.22E + 07	0	0.00061	0.00284
			Combined Failure Rate:		0.01261	0.02879
				FITs:	126.1	287.9

VAF = Voltage Acceleration Factor of 55

Failure Analysis:
A. Input leakage; no physical failure analysis performed.

SAN040147

APPENDIX A
FAILURE RATE CALCULATIONS FOR 60% UPPER CONFIDENCE LEVEL

Step 1. Accumulate data from 48 hours of burn-in through lifetest of each lot. (Note: 48-hour burn-in results measure infant mortality and are not included in the failure rate calculation.)

Step 2. Determine the failure rate mechanism for each failure and assign an activation energy (E_A) corresponding to each failure mechanism. (See Table 1 below.)

Table 1. Failure Mechanisms Activation Energies Relevent to ETOX™ Flash Memories

Failure Mode	Activation Energy
Defective Big Charge Gain/Loss	0.6 eV
Oxide Breakdown	0.3 eV
Silicon Defects	0.3 eV
Contamination	1.0 eV–1.2 eV
Intrinsic Charge Loss	1.4 eV

Step 3. Calculate the total number of device hours from 48 hours of burn-in through lifetest.

Example: 125°C Burn-In/Lifetest and a 2 lot sample

$$\frac{\text{\# failures}}{\text{total \# devices}}$$

	48 Hours	168 Hours	500 Hours	1K Hours	2K Hours
Lot #1	0/1000	1/1000	0/999	0/998	0/994
Lot #2	0/221	0/201	1/201	1/100	0/99
Totals	0/1221	1/1201	1/1200	1/1098	0/1093

Device Hours = (Number of Devices) (Number of Hours)

Total Device Hours = 1201 (168 hrs − 48 hrs) + 1200 (500 hrs − 168 hrs)

+ 1098 (1000 hrs − 500 hrs) + 1093 (2000 hrs − 1000 hrs)

= 1201 (120 hrs) + 1200 (332) + 1098 (500 hrs)

+ 1093 (1000 hrs)

= 2.185×10^6 Device Hours

SAN040148

Step 4. Use E_A tables to find the equivalent device hours at a desired temperature for each activation energy (failure mechanism), or use the Arrhenius relation.

$$R = A \exp\left[\frac{-E_A}{KT}\right]$$

K = 8.617×10^{-5} eV/°K (Boltzman's Constant)
A = proportionality constant
R = mean rate to failure
E_A = activation energy
T = Temperature in Kelvin

$$\frac{R_1}{R_2} = \frac{A_1 \exp\left[\frac{-E_A}{KT_1}\right]}{A_2 \exp\left[\frac{-E_A}{KT_2}\right]} = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

Where $A_1 = A_2 = A$ for the same failure mechanism (i.e., same E_A)

Where R_1 and R_2 are rates for a normal operating temperature and an elevated temperature respectively

$$R_1 = R_2 \times \exp\left[\frac{E_A}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

However, since rate (R) has the units $\left(\frac{1}{\text{time}}\right)$, we can think in terms of time to one failure or MTBF.

Thus,

$$R_1 = \frac{1}{t_1} \quad \text{where } t_1 = \text{MTBF at same temperature } T_1$$

and

$$R_2 = \frac{1}{t_2} \quad \text{where } t_2 = \text{MTBF at same temperature } T_2$$

Thus the Arrhenius Relation becomes:

$$\frac{1}{t_1} = \frac{1}{t_2} \times \exp\left[\frac{E_A}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

or

$$t_1 = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \times t_2$$

We then define the Acceleration Factor as:

$$A.F. = \frac{t_1}{t_2} = \exp\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

For example: For $E_A = 0.6$ eV, $T_2 = 398$°K, $T_1 = 328$°K

$$t_1 = 41.7\, t_2$$

Therefore, one hour at 125°C is the equivalent to 41.7 hours at 55°C for a failure mechanism of activation energy $E_A = 0.6$ eV. Then 41.7 is the thermal acceleration factor for time.

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NOTE:
The Arrhenius Plot is simply ln (Acceleration Factor) vs. 1/Temperature normalized for an MTBF (t_2) of one hour at 250°C (T_2). This plot can also be used to determine the acceleration factor between two temperatures (other than 250°C).

For example: For a 0.3 eV failure at 125°C, the acceleration factor is 8.1 relative to a 0.3 eV failure at 250°C. For a 0.3 eV failure at 25°C, the acceleration factor is 152 relative to 250°C. Therefore, the acceleration factor between 125°C and 25°C is:

$$A.F. = \frac{t_1}{t_2} = \frac{152}{8.1} = 18.7$$

Step 5. Organize the burn-in/lifetest data by E_A, Total Device Hours at the burn-in/lifetest temperature T_2, Thermal Acceleration Factors for each failure mechanism (E_A), Number of Failures for each failure mechanism, and the calculated equivalent device hours at the desired operating temperature T_1.

NOTE:
The rise in junction temperature due to the thermal resistivity of the package (θ_{JA}) must be added to the desired and actual burn-in/lifetest temperatures.

$$T_{test} = T_J - T_A = \theta_{JA}(IV @ T_A) - T_A$$

E_A (eV)	Total Device Hrs @ T_2	Acceleration Factors	# Fail	Equivalent Hours @ T_1
0.3	T.D.H.	X	N_1	X (T.D.H.)
0.6	T.D.H.	Y	N_2	Y (T.D.H.)
1.0	T.D.H.	Z	N_3	Z (T.D.H.)

The failure rates for individual failure mechanisms and the total combined failure rate can be predicted using the data table and the following formula:

$$\%\ fail/1K\ hrs. = \frac{\chi^2(n, \alpha)}{2T}(10^5)$$

Where $\chi^2(n, \alpha)$ is the value of the chi squared distribution for n degrees of freedom and confidence level of α. T is the total equivalent device hours at T_1. The total combined rate is just the sum of the individual failure rates for each failure mechanism.

For a 60% UCL, the above formula converts to the following:

# Failures	% fail/1K hours 60% UCL
0	$0.915 \times 10^5/T$
1	$2.02 \times 10^5/T$
2	$3.105 \times 10^5/T$
3	$4.17 \times 10^5/T$
$3 < \# < 15$	$\frac{1.049(\#\ failures\ for\ a\ particular\ E_A) + 1.0305}{Equivalent\ hours\ @\ T_1}\left[10^5\right]$
> 15	$\frac{(0.2533 + \sqrt{(4 \times \#\ failed) + 3})^2}{4T}\left[10^5\right]$

SAN040150

An In-System Reprogrammable 256K CMOS Flash Memory

SESSION X: NONVOLATILE MEMORIES

SAN040168

THAM 10.7: An In-System Reprogrammable 256K CMOS Flash Memory

Virgil Niles Kynett, Alan Baker, Mick Fandrich, George Hoekstra, Owen Jungroth, Jerry Kreifels, Steven Wells
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ADVANCES in TUNNEL OXIDES have made it possible to develop a 256Kb double-poly, single-transistor, electrically erasable, programmable flash memory. The device is a high-density nonvolatile flash memory optimized for microprocessor-controlled reprogramming capability. Using advanced CMOS 1.5μm technology, a 192mil square, 32,768 x 8b device has been designed with a 6μm x 6μm cell. Figure 1. The memory has a 110ns access time with a 200ms electrical erase time, and a 100μs/byte program time. Figure 2. Using CMOS inputs, dissipation is 150mW in the active state and 0.50mW in the standby mode.

Based on EPROM technology, the cell used the same programming mechanism, but can be electrically erased, achieved by using a tunnel oxide under a single transistor floating poly gate cell. The flash cell requires a 12V power supply for erase and program. The erase mechanism utilizes Fowler-Nordheim tunneling to move electrons from the floating gate to the cell source junction. Programming is achieved in the standard EPROM manner of hot electron injection from the cell drain junction to the floating gate.

Reduced electric field across the tunnel Oxide has improved reliability. The flash requirements are 12V for erase and program, as opposed to 18V needed for FLOTOX technology. No oxide breakdown has appeared in over more than 10,000 erase program cycles. The primary limitation to flash cell cycling is an increase in erase and program time caused by electron and hole trapping in the tunnel oxide.

Command port architecture has been used in the design to afford microprocessor control of program, erase, program verify, erase verify, and read modes without the need for additional or high-voltage multiplexed pins. On-chip address and data latches minimize system interface logic. A 12V program and erase voltage, required on the VPP supply pin for reprogramming, enables the command port. The command port is disabled by bringing V_{PP} to 5V, allowing standard EPROM read operation.

Functions are selected via the command port in a write cycle controlled by th $\overline{WE}$ and $\overline{CE}$ pins: Figure 4. Contents of the address register are updated on the falling edge of $\overline{WE}$. The rising edge of $\overline{WE}$ latches the command register and the data register, decodes new internal modes, and initiates operations. Verify voltages derived from VPP are applied to the wordlines through the X-decoder during program verify and erase verify to guarantee program and erase margin.

Erase is achieved by a two-write sequence with the erase code written to the command register on the first write cycle, and the erase confirm code written on the second cycle. The confirm code initiates erase upon the rising edge of $\overline{WE}$. The command decoder triggers a high-voltage switch connecting 12V to all array cells and grounding all wordlines. Fower-Nordheim tunneling results in a simultaneous erase of all array cells. Writing the erase verify code to the command register terminates erase, latches the address of the byte to verify, and sets up internal erase margin voltages. A microprocessor can then access the output from the addressed byte using standard read timings. Verify procedure is repeated for all addresses.

Programming is executed in a similar manner. The program command is entered in the command register on the first occurrence of WE low. A second WE cycle is then required to load the address and data latches. The second write initiates programming by applying high voltage to the gate and drain of the addressed byte. Writing the program verify command terminates programming and sets internal margin voltages to verify the newly programmed byte. Addressed byte can be accessed using standard microprocessor read timing .

A pair of circuits generate erase verify and program verify voltages on-chip. Figure 5. A high-voltage switch (transistors M1-M4) disconnects V_{pp} from the resistor when not in verify mode. Matched transistors M5 and M6 form a buffer driving the large internal capacitance with the voltage.

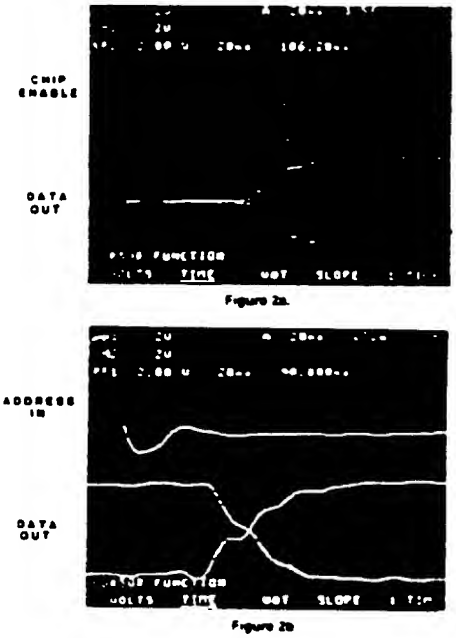

FIGURE 2 – T_{CE} chip enable access time *(a)*, T_{ACC} address access time *(b)*.

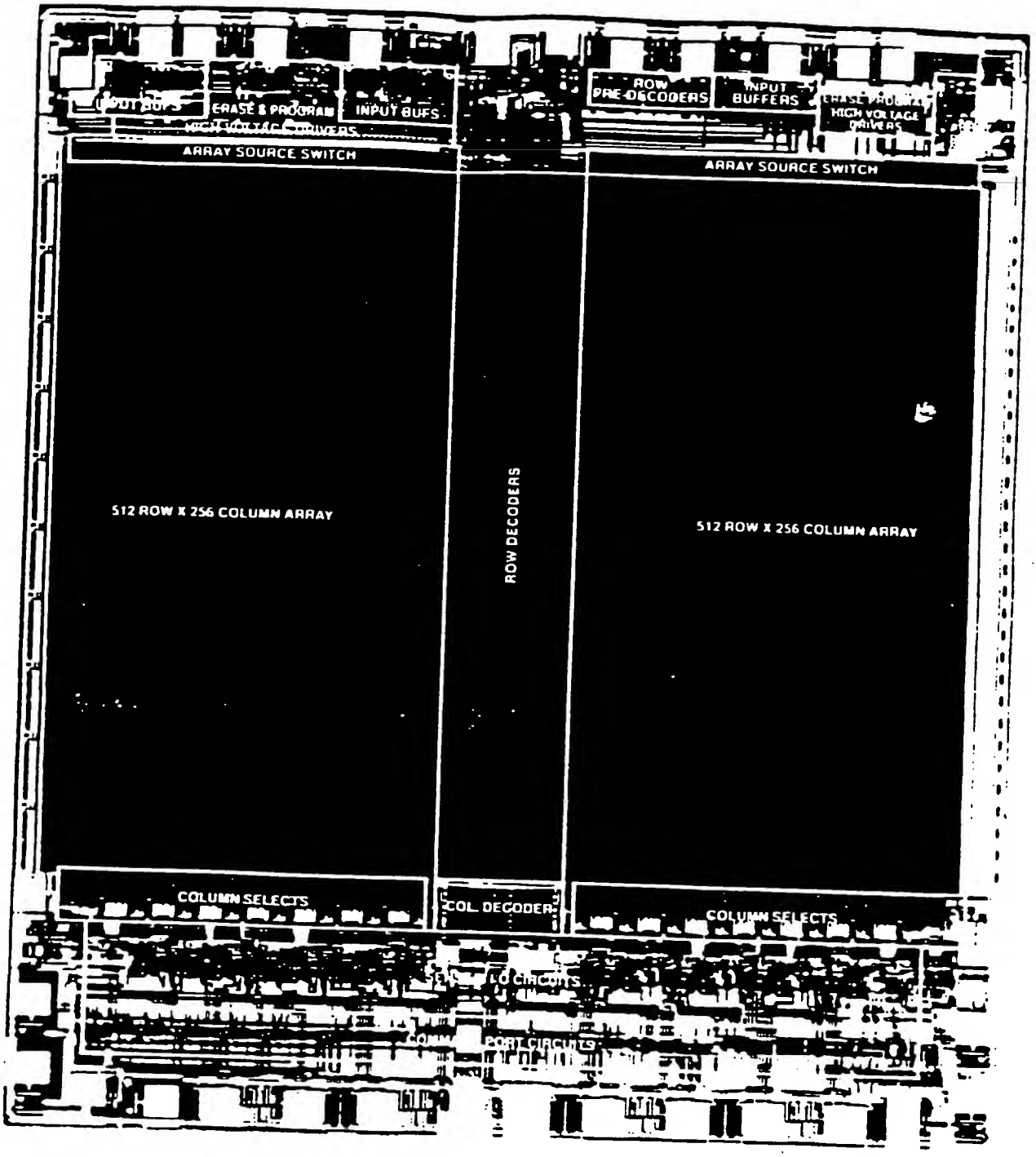

FIGURE 2 – 256Kb flash memory die.

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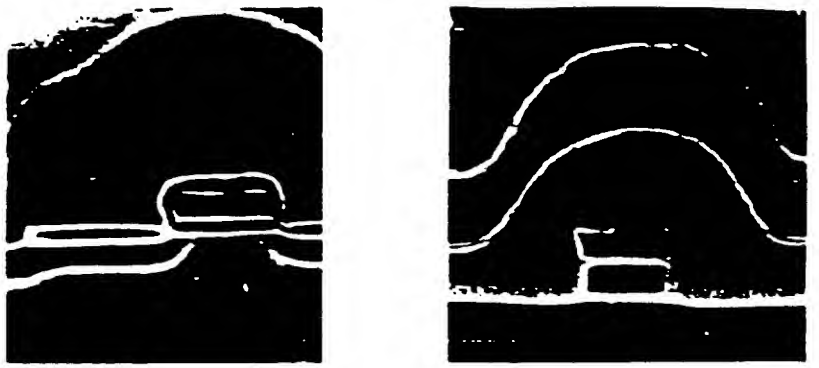

a) CMOS Flash cell.
(10,000 x magnification)

b) CMOS EPROM cell.
(10,000 x magnification)

FIGURE 3 – CMOS flash memory cell vs. CMOS EPROM cell cross-section. Both are 10,000 x magnification.

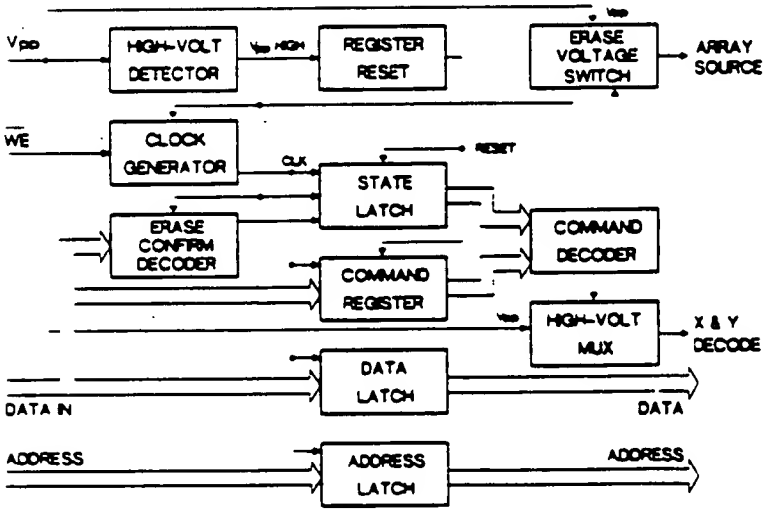

FIGURE 4 – Command port schematic.

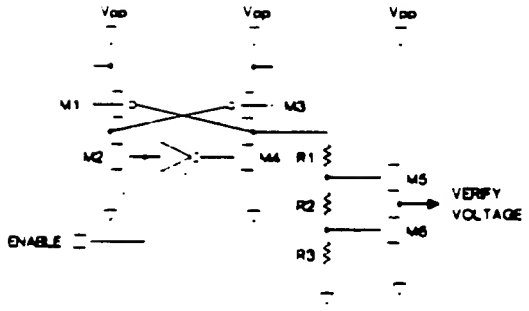

FIGURE 5 – Erase/program verify circuit.

Technology	Cell	Periphery	Device	
1 Sum Lithography	Area = 6um x 6um	HMOS-II	Die Size	387.43 mils
Double-Polysilicon	Gate 1 = Tunnel Oxide	T_{ox} = 400Å	Organized	32768 x 8
N-well CMOS	T_{erase} = 200ms	L_{eff} N-ch = 1.4um	Supply Voltage	V_{CC} = 5V
	$T_{program}$ = 100us	X_j = 0.3um		V_{PP} = 12V
	Read Current = 100uA	X_d = 0.4um	Active Power Dissipation	160mW
			Standby Power Dissipation	0.55mW
			Chip Enable Access Time	110ns
			Operation	Asynchronous

TABLE 1 – Device parameters.

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Cost-Effective Field Reprogrammable Code – Flash Memory Technology

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ABSTRACT

"Flash" nonvolatile memory technology, unleashes new power for automotive electronics. It provides field reprogrammability at a fraction of the cost of conventional E^2PROM due to its similarity to the cost-effective EPROM. It is now feasible for control programs to be modified over time as dictated by vehicle wear. The designer can implement systems which are modified via external interface or even create "intelligent" self-reprogrammed machines.

INTELLIGENT SYSTEMS COME OF AGE

Advances in semiconductor technology have rapidly propelled automotive electronics through distinct stages of development. The technologies and capabilities they afford are closely linked. The first stage was characterized by discrete transistors, diodes, and simple analog circuits. It produced alternator rectifiers and electronic ignition under the hood as well as solid-state radio, cruise control, and digital clocks for the driver's convenience. The second phase, initiated by 4- and 8-bit microprocessors in the late 70's, brought more sophisticated ignition and emission control, anti-lock braking, and, more recently, active suspension.

The next era of automotive electronics promises significant enhancements to both vehicle performance and driver amenities. Advanced powertrain, suspension, and braking control in fully integrated systems can optimize engine performance and vehicle control with unprecedented smoothness and safety. What is the makeup of such systems? "Smart" power and sensing devices, 16- and 32-bit microprocessors, and large amounts of electrically reprogrammable memory are the building blocks of this expanded automotive intelligence (Figure 1).

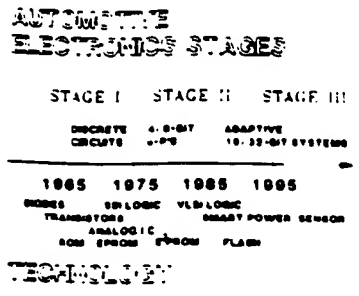


Figure 1. Technology and Stages of Automotive Electronics Development

Earlier automotive microprocessors often employed mask-programmed ROMs (MROMs) in 8 K-byte and lower densities. Now the EPROM technology in 32 K-byte density has become commonplace. Why? Higher density is an obvious requirement of more sophisticated control functionality, driven by processors with expanded word-widths, instruction sets, and I/O capabilities. The use of EPROM results from: 1) the increased probability of a need for code modifications as a function of higher density memory itself, and 2) the flexibility advantage over MROM. Since mask-programmed ROMs are coded by the semiconductor manufacturer, the automotive user must forecast the desired mix of MROM codes well in advance of shipping a finished vehicle, then depend on the MROM vendor to deliver on each MROM type. In contrast, the user codes EPROMs. The electronics assembler carries one type of inventory for all needs and has the flexibility of customizing each electronic control module for its designated vehicle.

The user can precisely match the output of EPROM codes to assembled vehicles. Auto makers now exploit this capability to differentiate engine control options among product line offerings.

If the EPROM's factory programming capability is so desirable, what could the automotive industry do with field-reprogrammable devices? A simple answer to that question is another question: If an engine performance changes as it wears, should its control program change with it? The answer is yes. In fact, it is likely that environmental regulations will require alterable code, demanding electrically erasable memories. In this case, the ignition and emission control programs would be modified over the life of the vehicle (Figure 2).

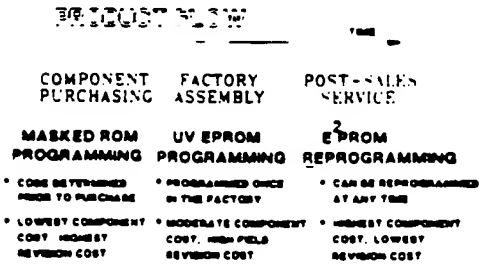


Figure 2. Memory Technology Flexibility Versus Automotive Application Need

Next-generation control modules will not only need field-reprogrammable memories, but very dense memories as well. The new automotive memory targets are 64 K-byte and 128 K-byte (1 megabit) densities. While 128 K-byte EPROMs have shipped in volume for over a year, they are not electrically erasable. E^2PROMs have just now reached the 32 K-byte density, falling short of the emerging need.

There has been a gap in nonvolatile memory technology. EPROMs have met the need for high density, but ultraviolet light erasure complicates reprogramming. Conventional E^2PROM has electrical erasure yet lacks density. The automotive industry's ever-increasing electronic complexity makes new demands on memory technology. Post-sales code modification is becoming a requirement. Electronic modules need EPROM density and electrical erasure together! Fortunately, the key to the memory capability demanded by cars of the future has just arrived: *Flash memory technology*.

FLASH TECHNOLOGY: THE KEY TO LARGE, REPROGRAMMABLE MEMORIES

Flash is the newest nonvolatile memory technology. Closely resembling its sibling, the EPROM, Flash provides electrical erasure and high device density. In fact, the approach taken by Intel Corporation results in a Flash memory cell identical in size to the EPROM. In contrast, conventional E^2PROM cells are typically two to three times larger than Intel's Flash or EPROM cells produced with the same photolithography (Figure 3). The implication is that Flash memory adds the critical functionality of E^2PROM with storage capacity and reliability equivalent to EPROM.

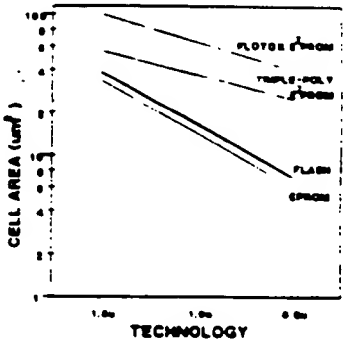
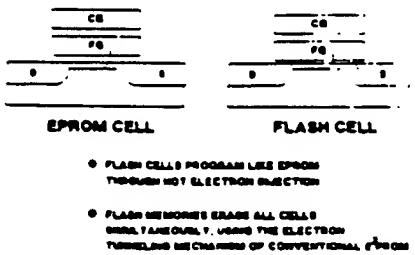


Figure 3. NonVolatile Technologies Versus Photolithography

HOW FLASH WORKS

Intel Corporation has recently developed a Flash memory cell based on its CHMOS II-E EPROM technology. Using standard self-aligned EPROM floating and control gates, the fundamental difference is a thinner first gate oxide (Figure 4). This thin oxide beneath the floating gate enables electrical erasure.



- FLASH CELLS PROGRAM LIKE EPROM THROUGH HOT ELECTRON INJECTION
- FLASH MEMORIES ERASE ALL CELLS SIMULTANEOUSLY, USING THE ELECTRON TUNNELING MECHANISM OF CONVENTIONAL E²PROM

Figure 4. Comparison of EPROM and Flash Memory Cells

* CHMOS is a patented process of Intel Corporation.

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Hot electron injection causes programming when the drain and control gate are connected to high voltage, the identical mechanism to EPROM. Electrons deposited on the floating gate raise the cell threshold, resulting in the programmed state. While EPROMs rely on ultraviolet light to remove electrons, Flash memories erase through the Fowler-Nordheim tunneling mechanism used in byte-alterable E²PROMs.

The electric field driving Flash tunneling is created by a high source voltage, grounded control gate, and disconnected drain. All cells erase simultaneously through their common source. Flash differs from E²PROM in cell size and erase functionality. Larger E²PROM cell sizes arise from extra components required for individual byte erasability. Examples are the third gate of triple-poly or the second transistors of Flotox and MNOS E²PROM technologies. Larger cell size, hence lower device density, is the price of byte-alterable functionality.

APPLICATIONS MATCHING MEMORY FORM AND FUNCTION

Automotive applications utilize various memory technologies. Static RAM handles the need for a data manipulation "scratchpad." The density requirement is often small enough to be integrated onto the CPU chip. Most of the external memory, on the other hand, provides nonvolatile code storage. The growth in code density in the automotive world drives large, off-chip memory needs. Also, increasing controller complexity translates to larger CPU die size and even more memory usage; functionality offsets integration gained from advances in semiconductor photolithography. Thus, the nonvolatile memory remains off-chip. The designer, in turn, can choose the code memory type which best suits the application needs.

"You get what you pay for" is as true in nonvolatile memories as anything else. We have already discussed ROM, EPROM, Flash, and E²PROM in the contexts of cell sizes and flexibility. Figure 5 illustrates this cost and function hierarchy.

ROM provides lowest cost in very stable applications that do not require code modification. Next EPROM, then Flash, increase functionality at equivalent densities. Finally, E²PROM provides highest functionality, but carries a substantial cost and density penalty. These technologies fit uniquely into application need categories.

Advanced electronics already reside in three primary application categories: 1) powertrain, 2) chassis, and 3) information & body computer. Engine management and electronic transmission systems are in production. So are anti-skid braking, shock damping, and four-wheel steering. The cockpit can have climate and cruise control, infrared door locking, air bags, and service diagnostic computers.

The 1990's will bring powertrains with continuously variable transmission, traction control, then fully-active suspension, and sophisticated information systems such as navigation, collision avoidance, and "heads-up displays."

Again, functional complexity drives the processor and memory requirements. Figure 6 gives examples of these relationships. ROM usage corresponds to stable, low-density code, typically integrated with the controller. Flash, however, is redrawing the other nonvolatile memory lines.

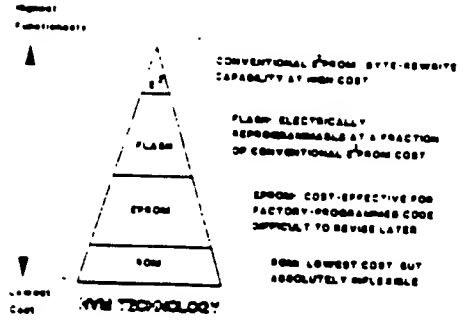

Figure 5. The Nonvolatile Memory Hierarchy

APPLICATION CATEGORY	COMPUTER CONFIGURATION: PROCESSOR NEEDS	COMPUTER CONFIGURATION: MEMORY NEEDS
POWER-TRAIN	8- TO 32-BIT CPUs	8- TO 64-BYTES EPROM up TO 256-BYTES E²PROM
CHASSIS	8- TO 32-BIT CPUs	8- TO 16-BYTES EPROM up TO 256-BYTES E²PROM (FOR ACTIVE SUSPENSION ONLY)
INFO/ DISPLAY	4- OR 8-BIT CPU (MONOLITHIC)	4-BYTES ON-CHIP ROM up TO 256 BYTES ON-CHIP E²PROM
BODY/ COCKPIT	4- OR 8-BIT CPU (MONOLITHIC)	4- TO 64-BYTES ON-CHIP ROM

Figure 6. Application, CPU, and Memory Relationships

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Since Flash technology is new, it forces a new perspective. It will reside where EPROM or E²PROM are used today. Where EPROM provides flexibility in the factory, Flash extends it beyond the assembly line. Where E²PROM allows modification of code and large data bases, Flash yields a denser, cheaper solution.

Flash is a viable alternative for many of the automotive EPROMs in use today. Code modification is a powerful capability for post-sales service. Flash also impacts E²PROM. The number of parameters requiring individual byte manipulation in "real time," while the vehicle is in operation, is often quite small. Accordingly, byte-alterable E²PROM has been employed in some cases where that functionality is not really needed. Flash allows more cost-effective employment of E²PROM, concentrating it where it is needed. Figure 7 maps these new nonvolatile memory boundaries onto the emerging applications.

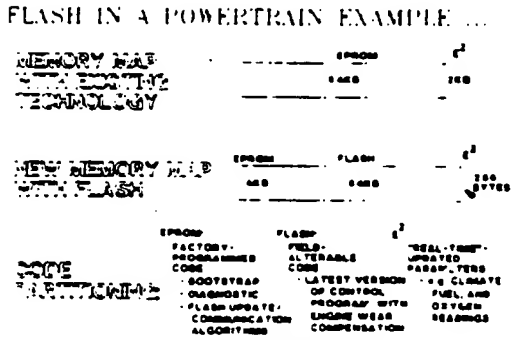

Figure 7. The New Flash Partition Emerging in NonVolatile Memory Applications

DESIGNING IN A FLASH

From a technology qualification standpoint, Flash reliability will be assessed via proven EPROM test methods during the next few years. Initial evaluations bear out the EPROM reliability analogy; Flash failure rates, like EPROM, are significantly lower than E²PROM. The new functionality "standpoint," however, is different. Flash implementation involves changes in both manufacturing and services. New equipment and methods all demand particular attention.

Today's electronic modules are quite capable of reprogramming themselves, given that they incorporate Flash. While this may be an ultimate goal, the acceptance of such a development may take time. Initial Flash applications, like the testing, will also borrow EPROM concepts. Thus, new technology adoption is a gradual extension of proven methods.

The first automotive microcomputers employing Flash will likely receive new code during maintenance service. Performance or emission measurements might be taken, then custom-tailored code revisions developed by a host computer. This host would have the same capabilites as standard EPROM programming equipment. Simply plugging this machine into the microcomputer permits Flash reprogramming. Removing the programming voltage source gives absolute insurance against code disruption. All system modification is done in a controlled, factory-authorized environment.

Present manufacturing techniques lay the foundation for Flash. Compact, surface-mount packaging is accelerating a trend toward programming EPROMs "on-board." On-board programming allows full module assembly with non-coded memories. A single, reduced board run-rate services the entire factory output since coding can be done "just in time," i.e. at the end of the assembly line. Flash-based syetems can immediately use this same capability for field service (Figure 8). Rapid factory reprogramming also enhances testing and quality.

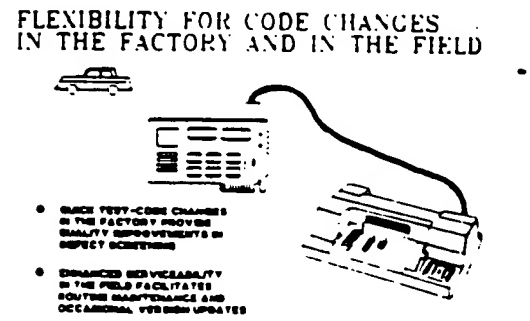

Figure 8. Flash Memory Updates Made Easy With On-Board-Programming Techniques

"FLASH FOWARD"

Future implementations of Flash will further exploit the technology's capabilities. Simple chip circuits can handle the need for special reprogramming voltages, all from a fixed programming power supply. The local microprocessor, rather than an external EPROM programmer, can administer the Flash reprogramming. This opens two new avenues: 1) the ability to update code from a serial communication link, and 2) the ability for the vehicle to routinely update itself.

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Flash technology resembles EPROM closely, giving users confidence that it can meet the automotive industry's high standards of quality and reliability. It will prove itself in field service applications. The serial communication capability enhances serviceability without compromising reliability. Each development phase becomes a stepping stone for the next; self-reprogramming systems are not a far stretch from serial communication (the programming supply and supervisory intelligence are local in both, and self-reprogramming could be triggered by the odometer to occur the next time the vehicle is turned off!). In any case, a conservative 100-cycle reprogramming specification is a big first step: a control system could be fine-tuned every 2,500 miles for a 250,000-mile engine and powertrain lifetime.

Extended capability should open even more possibilities. Intel's Flash memories have demonstrated reliable operation to well over ten thousand cycles. The best part about Flash is that it is not just theory. It is here now. For meeting the needs of alterable electronics, we are now limited only by our development capabilities, not those of programmable memory.

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SAN040175

A 90ns 100K Erase/ Program Cycle Megabit Flash Memory

by Virgil Niles Kynett, Jim Anderson, Greg Atwood, Pat Dix, Mick Fandrich, Owen Jungroth, Susan Kao, Jerry A. Kreifels, Stefan Lai, Ho-Chun Liou, Benedict Liu, Richard Lodenquai, Weh-Juei Lu, Roy Pavloff, Daniel Tang, J.C. Tzeng, George Tsau, Branislav Vajdic, Gautam Verma, Simon Wang, Steven Wells, Mark Winston, and Lisa Yang

ABSTRACT

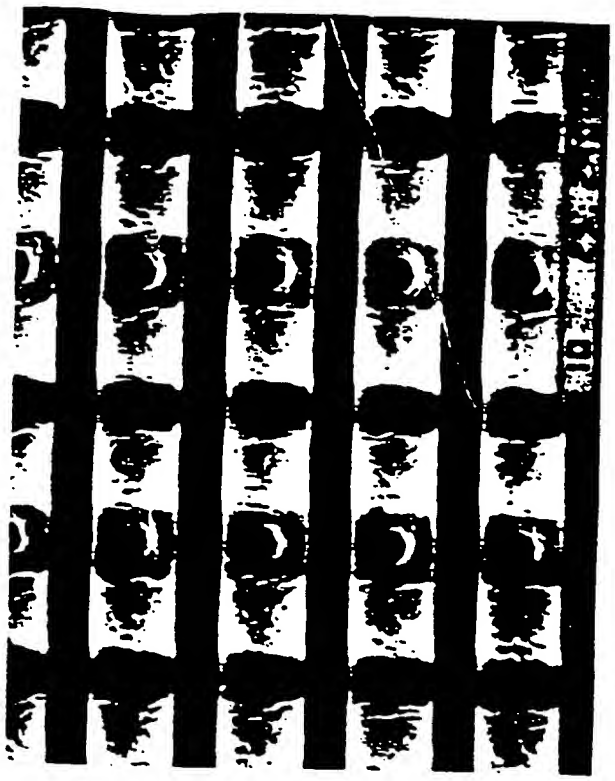
Using advanced 1.0μm CMOS technology, a 245 mil square 131072 × 8 device has been fabricated with a 3.8μm × 4.0μm cell. The memory exhibits a 90ns read access time with a 900ms electrical array erase and 10μs/byte program time. The device has been optimized for in-system microprocessor-controlled reprogramming with endurance performance greater than 100,000 erase/program cycles. Column redundancy is implemented with the utilization of flash memory cells to store repaired addresses.

ADVANCES in photolithography have made it possible to develop an electrically erasable reprogrammable 90ns 1Mb flash memory which is capable of greater than 100,000 erase/program cycles. This 1Mb memory implements a command port and an internal reference voltage generator, allowing microprocessor-controlled reprogramming [1].

The 90ns access time results from a high memory cell current (95μA), low resistance poly-silicide wordlines, advanced scaled periphery transistors, and a di/dt optimized data-out buffer. Using CMOS inputs, power dissipation is 40mW in the active state and 20μW in the standby mode. The memory electrically erases in 900ms and programs at the rate of 10μs/byte. The device contains thirty-two columns of redundant elements and utilizes flash memory cells to store the address of repaired columns. The use of the flash memory cell reduces the required silicon area significantly over the commonly found large metal-shielded EPROM cells [2].

The 1Mb flash memory was fabricated on a 1.0μm double poly n-well CMOS process. Silicide was utilized on the wordlines to help achieve the 90ns access time performance. The CMOS periphery circuits were constructed with 0.9μm L_{eff}, 250 Å gate oxide LDD transistors. The density of this 1μm flash technology is demonstrated on the 1.0μm and 1.5μm memory cell comparison shown in Figure 1. The 1.0μm memory cell has a 15.2μm² area, which is over twice as small as the 1.5μm memory cell. A microphotograph of the 245 mil², 128K × 8 flash memory is shown in Figure 2. The process/device characteristics are summarized in Table 1.

a) 1.5μ Lithography
(5,000 x magnification)



b) 1.0μ Lithography
(5,000 x magnification)

Figure 1. Array SEM microphotograph: (a) 1.5μm memory cell (6μ × 6μ) (b) 1.0μm memory cell (3.8μ × 4μ)

One of the most significant aspects of this device is its 100,000-cycle capability. A typical cell erase program Vt margin is shown as a function of reprogramming cycles in Figure 3. After 100,000 cycles there still exists a 2.5V program read margin to insure reliable data retention. Accelerated retention bake experiments done at 250°C for 168 hours indicate that after 10,000 cycles the memory will exhibit only 0.7V program Vt shift. Program and erase time degrade slightly due to normal charge trap-up in the tunnel oxide (Figure 4). In addition, endurance reliability has been excellent with no tunnel oxide breakdown.

Table 1. Device Parameters

Technology	Cell	Periphery	Device
1.0-μm Lithography	Area = 3.8μm × 4μm	Tox = 250 Å	Die Size: 60116 mils²
1-Poly, 1-Silicide	Gate Oxide > 100 Å	Leff N – P = 0.9μm	Organized: 128K × 8
N-Well CMOS	Read Current = 95μA	Xjn = 0.3μm	Access Time: 90ns
Edi on P–	Terase = 900ms	Xjp = 0.6μm	Active Power: 8mA
	Tprog = 10μs/byte		Standby Power: 4μA
			Package: 32-pin Cerdip

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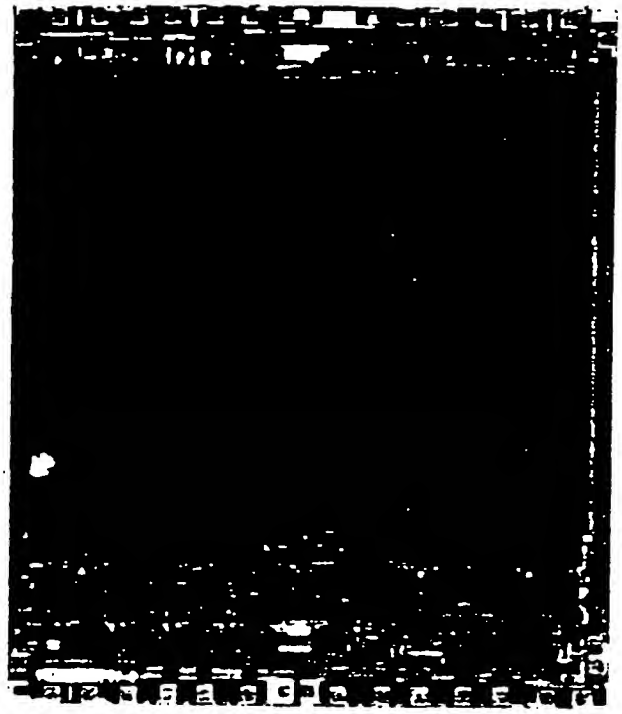

Figure 2. 1Mb die photograph

However, to build a manufacturable 1Mb flash memory, it is essential to be able to control the memory array erase Vt. The key is the proper selection of the erase Vt maximum and maintenance of a tight Vt distribution. The maximum erased Vt is set to 3.2V via the erase algorithm and the internal erase verify circuits [3]. Good oxide quality gives an erased Vt distribution width that does not change appreciably with cycling (Figure 5). The tight erase Vt distribution gives an order of magnitude of erase time margin to the fastest erasing cell (Figure 6).

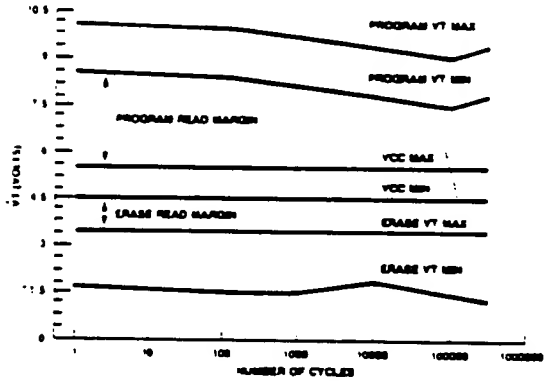

Figure 3. Array Vt vs. cyles

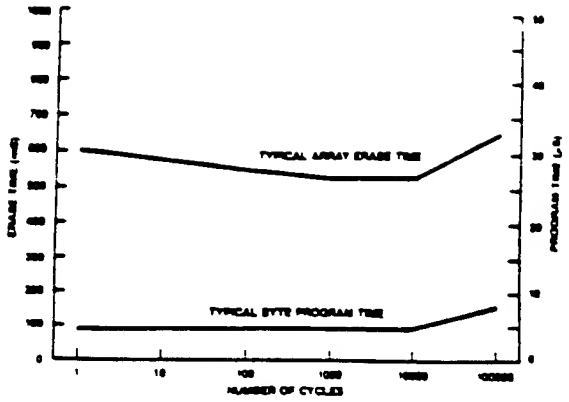

Figure 4. Erase/program time vs. cycling

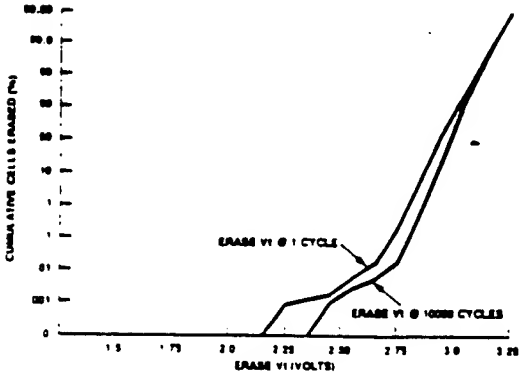

Figure 5. Erase Vt distribution vs. cycling

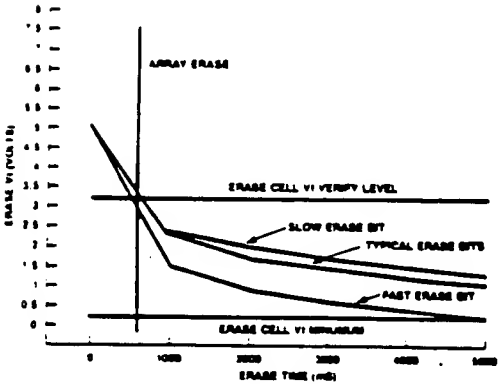

Figure 6. Array erase Vt profile vs. erase time

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Array erase is executed by switching high voltage onto the source junction of all cells and grounding all select lines. The array source switch, shown in Figure 7, switches high voltage onto the source junctions. Transistor M16 is a very large device which pulls the source to ground during read and program modes. During erase mode, the high voltage latch formed by M5-M8 enables transistor M15, which then pulls the array source up to 12V. To obtain fast array erase times, this device must be made large enough to supply the grounded gate breakdown current which occurs on the sources of the memory array. The upper boundary on M15 current sourcing capability is set by the maximum allowable substrate current. If VPP is raised to 12V before VCC is above approximately 1.8V, the low VCC detect circuit formed by M1-M4 drives the node LOWVCC to 9V. Transistors M9-M11 then force the erase circuit into a non-erase state with M15 off and M16 on. When VCC rises above 1.8V, the chip will be reset into a read state.

Redundancy circuits consist of two flash memory cells combined with a cross-coupled bias and sense circuit ensuring low power consumption (Figure 8). When either M7 or M8 is programmed, the latch no longer draws power. By setting the levels of CLAMP and BIAS to Vt and 2Vt respectively, the B and BB levels are held to approximately one Vt. The signals F and FB along with the address signal drive the inputs to the XNOR circuits. The MATCH signals for all column addresses are combined to create the full match signal which enables a redundant column.

In summary, a 90ns 1Mb flash memory has been developed through the ability to scale the flash memory cell onto a standard CMOS 1.0um technology. This memory has been optimized for in-system microprocessor-controlled reprogramming for more than 100,000 erase, program cycles.

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2) G. Caneau et al., "A 90ns 4Mb CMOS EPROM," in ISSCC Dig. Tech. Papers, Feb. 1988, pp. 120-121, 323.
3) V. Kynett et al., "An In-System Reprogrammable 32K × 8 CMOS Flash Memory," IEEE J. Solid-State Circuits, vol. 23, pp. 1157-1163, Oct. 1988.

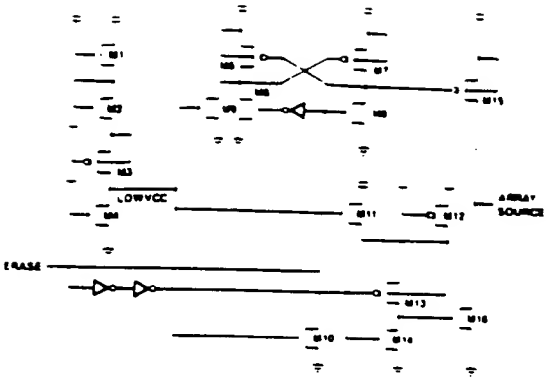

Figure 7. Array source switch

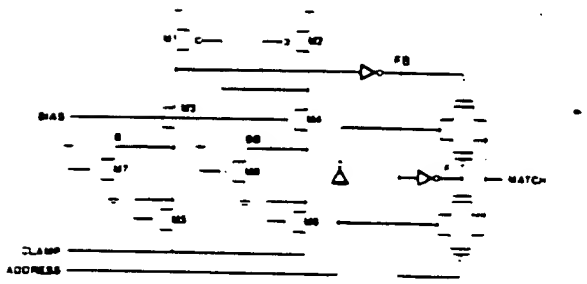

Figure 8. Redundancy circuits

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TECHNOLOGICAL

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Endurance Brightens the Future of Flash

Flash memory as a viable mass-storage alternative

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Imagine the ideal memory. It would be infinitely and randomly rewritable at static-RAM speeds and with dynamic-RAM capacity. All memory technologies in reality demand concessions from their users, and both ROM and RAM solutions incur higher system costs to circumvent their respective drawbacks. Various types of E²PROM and "shadow" NVRAM offer features closest to ideal, but at a lower density and higher cost than RAM.

The distinguishing characteristic of "RAM" is random write capability at read speeds (i.e. "symmetrical read/write"). The chief drawback of both dynamic- and static-RAM technologies is volatility. Typically, DRAM is backed by magnetic disk, while low-power CMOS SRAM is supported by auxiliary battery power.

In contrast, ROMs are inherently nonvolatile. They excel at storing code, as long as one does not need to change it. EPROMs offer more flexibility by allowing electrical reprogramming – after a long exposure to ultraviolet light performed outside of the computer system. EPROMs are generally treated as user programmable, but not reprogrammable. Frequently updated code creates logistical problems for EPROM users due to the cumbersome UV erase procedure.

Intel's ETOX™ flash technology could well strike the optimum balance between ROM and RAM. From a semiconductor processing standpoint, ETOX technology evolved from EPROM just as its acronym implies: "EPROM-Tunnel Oxide." It has the smallest read/write memory cell for any given photolithography and true nonvolatility, trading off fast rewrite for slower write and block-clear functionality. Based on observations of other electrically erasable (E²) technologies, ETOX has a theoretical limitation in the total number and success rate for successive erase/write operations, or write/cycle endurance. In actual practice, most applications exhibit virtually infinite endurance: no "hard" memory-cell failures due to catastrophic oxide breakdown have been seen on thousands of devices tested. Neither has the E² "window closing" wear-out effect been found significant after tens of thousands endurance of cycles.

Looking more closely at typical applications, even the most frequent code updates only number in the realm of tens per year. Also, code is updated "en masse", all at once. For these reasons, the functional tradeoffs (e.g. the lack of single-byte alterability) made by flash technology are not issues for code storage.

Data storage, on the other hand, automatically evokes the image of DRAM and disk. This results from the desire for very high capacity for archival data storage. Secondly, data is generally rewritten more frequently than code. Nonvolatile memories, namely E²PROMs, have struggled for years to improve write endurance. Ironically, the stated endurance ratings are not the primary issue. Closer inspection reveals that most systems typically need far fewer write cycles over their lifetimes than the number currently offered by chip makers.

The success rate for E²PROM cycling is the bigger issue. Failure rate specifications of up to 5% for 10,000 write cycles is common. Another limiter for widespread E²PROM or NVRAM adoption is low capacity arising from complex transistor structures and fabrication processes.

ETOX flash technology provides essential E²PROM capability with unprecedented density, quality, and reliability. Its simple, stacked-gate, one-transistor cell affords two to four times the capacity, or cost savings per bit, of comparable E²PROM technologies. Ninety-five-percent process compatibility with EPROM allows ETOX to tap a proven manufacturing base (Figure 1). Equally important is the ETOX breakthrough in high-quality cycling endurance: 10,000-cycle failure rates are specified at less than 0.1%, and endurance of well over 50,000 cycles is typical – without failures. Data retention and lifetime reliability statistics are equivalent to those of EPROM. Typical endurance far exceeds the E²PROM-standard 10,000-cycle minimum.

ETOX versus E²PROM

The E²PROM, like the EPROM, was invented by Intel in the 1970's. The principle of Fowler-Nordheim electron tunneling drives electrical erasure, eliminating the UV-erasure requirement of EPROM. ETOX flash memories are erased in the same way, but they use the EPROM's channel hot electron-injection (CHE) programming method. E²PROMs employ tunneling for both the write (program) and erase operations.

EPROM is programmed and erased by depositing and removing electrons from a "floating" gate. Floating-gate cells differ from normal transistors only in having an extra, unconnected gate sandwiched between the normal (control) gate and the channel region between the source and drain. The cell is turned on by the capacitive coupling between the gates, whereby the "floating" gate provides a gate voltage similar to that of a standard single-gate transistor. This is the case for an "erased" or "ones state" EPROM cell.

Programming the cell to the "zero" or "off" state deposits electrons on the floating gate, resulting in a net negative charge.

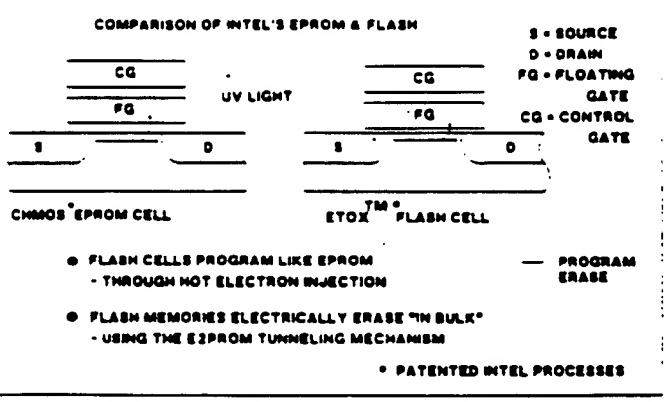

Figure 1: Intel's ETOX™ (EPROM-tunnel oxide) flash technology is 95% compatible with EPROM process technology. ETOX cells are programmed like EPROM, using channel hot-electron injection, and erased in bulk-erase fashion via the Fowler-Nordheim electron-tunneling mechanism used for E²PROM.

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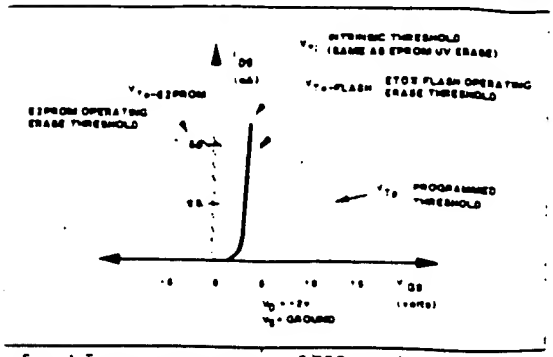

Figure 2: Tunneling erasure, used in both E²PROM and flash memory, is an active process, with the potential for producing negative erase thresholds. E²PROM's higher erasure voltage produces a wide scattering of cell thresholds.

The control gate must be taken to a much higher voltage in order to get a net floating-gate potential sufficient to turn the cell on. A typical off-state threshold voltage is 9 V or higher, versus the original on-state threshold of around 2 V. Within the standard logic voltage range, 0 to 5 V, an off-state cell cannot be turned on. The effect is identical to that of writing to a ROM, where a process masking step disables transistors for "zeros" coding.

The programmed EPROM cell is highly stable because a quantum-mechanical energy barrier holds the floating-gate charge. Only a high energy input can dislodge the excess electrons. This property provides nonvolatility—in contrast to the volatility inherent in DRAM because it has electrical connections through which its charge-storage capacitors leak. Both flash and byte-alterable E²PROMs are the same in this respect.

EPROMs employ ultraviolet light to supply sufficient energy to dissipate floating-gate electrons for erasure. This is a "passive", self-limiting process. UV erasure leaves the "intrinsic" amount of charge the floating gate had upon its creation. Thus, UV-erased cells have the same threshold voltage they had after initial wafer processing.

Tunnel erasure, used by both E²PROM and flash memory, is an active process, with erasure performed electrically through external control. The inverse of programming, erasure actively pulls electrons off the floating gates. When more electrons are removed than were added, leaving floating gate with less than the intrinsic number, cell thresholds go below their intrinsic level. If erasure is not carefully controlled, the highly efficient tunneling process can cause some cells to be erased very quickly, leaving some cells are depleted before others are sufficiently erased. (Figure 2 plots floating gate-transistor characteristics as a function of stored charge.) E²PROM's fast, higher-voltage erase procedure produces a wide scattering of cell thresholds. A threshold below 0 V creates an "always on" cell, or a depletion-mode transistor. Most of the E²PROM cell population ends up with negative thresholds after being erased, which in turn requires that extra transistors or control gates be employed to turn these cells off.

In contrast, ETOX flash combines lower-voltage operation with an advanced tunnel oxide process to implement controlled erasure. All cells tunnel-erase uniformly to produce a very tight cell threshold distribution very close to the UV-erase intrinsic threshold. ETOX technology produces the closest possible analogy to the UV-stimulated operation and compact cell size of EPROM. E²PROM's need for select devices adds to cell size, and hence cost. Figure 3 shows the program/erase mechanisms and compares the relative memory-cell sizes for ETOX flash and triple-poly E²PROM technologies.

The single-transistor barrier

E²PROM vendors have long sought to eliminate

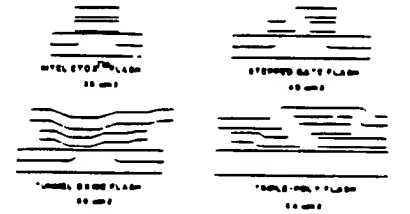

Figure 4: The ETOX cell's simple structure makes it smaller than other flash-type cells. This comparison is for a common 1.2-μm lithography.

the extra control gate or transistor for the obvious cost advantage this would bring. Ironically, the byte-alterability feature E²PROMs offer is made possible by the key barrier: single-byte erasure is facilitated by the deselect capability required for detaching erased cells from columns. Byte alterability also creates a performance constraint: If the contents of memory is changed one location at a time, the change must happen quickly for the chip-rewrite time to be reasonable. E²PROM makers commonly specify byte-rewrite times between 1 ms and 10 ms. The internal voltages used for these faster program/erase times are in the 20-V range, charge-pumped internally from the 5-V supply.

Since flash memories erase in bulk-array fashion, the per-bit time constraint is relaxed to thousands of milliseconds (i.e. seconds). (E²PROMs also have block-clear modes, but that does not remove the single-byte performance constraint.) Consequently, flash memories use a far lower internal erase voltage. This is a primary factor in erase control without control gates. Lower voltage also yields better reliability and cycling endurance. The 12-V supplies used with today's flash memories drastically reduce the electric field across the thin tunnel oxides inside each transistor, with the difference on the order of 2 MV/cm. This eliminates the catastrophic oxide-breakdown failures commonly observed in cycling of E²PROMs.

The ETOX cell's physical construction is another key reliability contributor. ETOX's EPROM-like structure allows defect-free oxide growth on undoped silicon. The cleaner oxide lacks the impurities linked to dopants. Furthermore, ETOX uses a small active tunnel oxide area, which results in fewer "active" defects and charge-trapping sights, and thus a reduced chance of failure. Since triple-poly E²PROM uses two oxide regions for tunneling, it has larger active area, as shown in Figure 3.

Other roads to flash

There are three keys to ETOX cell operation: 1) a very high-quality oxide, 2) unique drain and source structures, optimized for program and erase respectively, and 3) the use of complementary, adaptive program and erase algorithms. This combination supports well-controlled erasure and reprogramming of the simple stacked-gate ETOX cell.

The use of a truncated floating gate, or stepped-gate cell, also provides a flash E²PROM capability. The truncated floating gate's voltage must be accompanied by a select-gate voltage for turning on the cell. The programming operation and read function are identical to those used in EPROM and ETOX flash cells.

The stepped-gate structure's primary drawback is an electrical-stress-induced charge loss during programming known as "program disturb", whereby floating-gate charge is lost through the drain region of the cell. This and various other stresses are present with all floating-gate technologies and must be designed and processed out. Very tight stepped-gate process control can provide a sufficient "operating window", but in any case, electrical stresses are significant factors in cycle-related programming failures. Furthermore, the problem is exacerbated by slower programming, caused by a longer cell channel.

ETOX flash cells use separate program and erase junctions to ensure against these stresses. These separate operating regions are optimized for reprogramming speed.

Two other "flash" approaches have been developed. These are effectively hybrid technologies and have many of the same cost and reliability issues of

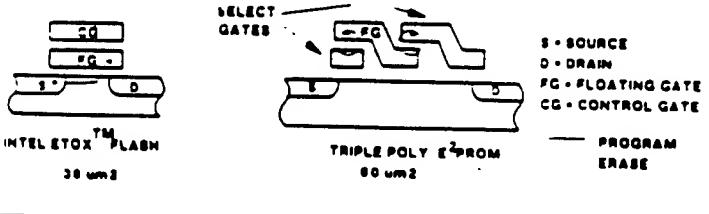

Figure 3: The ETOX cell is less complex and therefore smaller than the triple-poly E²PROM cell shown here for 1.2-μm lithography. The circle areas are the active tunnel regions. ETOX's smaller tunnel area reduces the chance of failure.

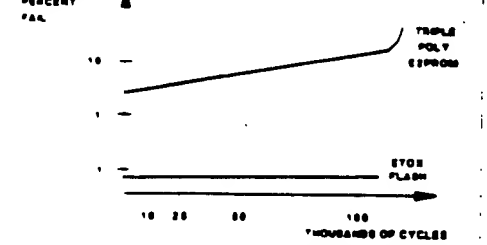

Figure 5: The failure rate of ETOX through 10 000 cycles is specified as less than 0.1% by statistical round-up from zero observed failures.

their byte-alterable E²PROM counterparts. Figure 4 shows what the relative cell sizes of all the "flash" technologies would be for a common 1.5-µm photolithography.

Endurance rooted in technology

Other functional differences aside, extended write cycling is important for both byte-alterable and flash E² memories. Various technologies all respond differently to this need. Conventional lifetest and data-retention reliability testing indicates dependability after successful reprogramming. This compares favorably among them all. The E²-specific need for cycling is where they differ.

Triple-poly E²PROMs have been observed to cycle well over the 10,000-cycle minimum before a substantial number of devices fail, with the failure rate remaining flat until catastrophic failure. When they do fail, triple-poly E²PROMs tend to fail from charge "trap-up". Like triple-poly, ETOX flash is theoretically trap-up limited but this has not caused failures in 256-kbit devices taken out to 100,000 cycles. (no data is available yet beyond that due to the newness of the technology). Most importantly, the failure rate of ETOX through the normal life of 10,000 cycles, specified as less than 0.1% by statistical round-up from zero observed failures, is substantially lower than that of byte-alterable E²PROMs (Figure 5). The triple-poly E²PROM cell has a much larger tunneling area exposed to high voltage compared to ETOX flash. Oxide breakdown is virtually nonexistent in ETOX flash compared with triple-poly E².

The lower voltages and relatively defect-free oxides used by ETOX memories prevent cycle-related damage. Trap-up causes a slowdown of the ETOX memory's program and erase operations as a function of cycling, but not hard failure.

Temperature and programming voltage (V_{pp}) also affect reprogramming rates. A 1-V change in V_{pp} makes almost an order-of-magnitude difference in program erase performance. Elevated temperature slows down programming (due to reduced carrier mobility) and speeds erasure. These effects are shown in Figure 6.

The programming-voltage effect explains Intel's different 256K product offerings. The 28F256 is available with either 12.0-V (± 5%) programming or an EPROM-compatible 12.75-V (± 0.25 V) programming voltage. The latter's worst-case V_{pp} is 1 V higher than the former's nominal V_{pp} to ensure successful reprogramming beyond the 10,000-cycle minimum. The 12.0-V version provides a minimum of 100 cycles to service designs with existing 12.0-V supplies. There is no difference in cycle-related failures, just in write performance. However, 12.0-V versions cycled over several thousand times may see a slowdown to where the reprogramming algorithms stop before erasure or programming is complete, but these are not hard failures.

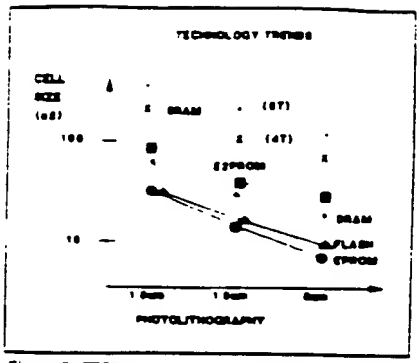

Figure 7: ETOX memory has the smallest read/write cell of any memory, including DRAM.

The volatile or nonvolatile choice

Many designers achieve system-level non-volatility using volatile-memory chips. Battery-backed SRAMs can provide a cost-effective solution in low-reliability environments. On the other hand, this is often unacceptable in reliability-critical environments. A battery is guaranteed to fail, and there are few reliable estimates as to when.

High-capacity systems often employ DRAM and magnetic or magneto-optical disks. Bulky, stationary equipment can employ disks without problems. Rugged, portable equipment cannot live with mechanical media like disks, at least not where a high degree of reliability is required. Electrically erasable memories, either flash or byte alterable, provide the ability to update their contents, along with ruggedness.

Designers have the hardest time choosing between alternatives where the reliability and density boundaries are less clear. For example, battery-backed SRAM is less expensive than flash due to greater volumes and cost learning. When ETOX flash hits mature volumes, it could easily be cheaper on a per-bit basis. In fact, ETOX memory has the smallest read/write cell of any memory, including DRAM (Figure 7). System-level costs for flash solutions are often cheaper than for disk-and-DRAM implementations — even though flash is more expensive on a per-bit basis — because the latter incur a fixed cost for the disk, independent of capacity. Since flash memory is added in single-component increments, it is cheaper overall than disk/DRAM up through a few megabytes of capacity (Figure 8). Furthermore, the cost crossover point between disk/DRAM and ETOX systems will increase because flash technology currently has a much steeper slope on its cost learning curve.

The primary barrier perceived by designers considering flash memory is cycle endurance. This issue deserves a closer look. Code storage for embedded controller programs or standard computer applications is infrequently updated; twenty-year system lifetimes rarely generate even 100 rewrites. The next level of write cycles is seen in routinely-changed data tables. Examples include updates to navigational-computer parameters, black-box recorders, or even automobile-engine parameters that can be modified for changes in the composition of each tank of gas. These data, changed typically on a weekly basis, require about 1000 write cycles over a twenty-year period.

One might think that archival data storage in general-purpose computers must exceed ETOX write

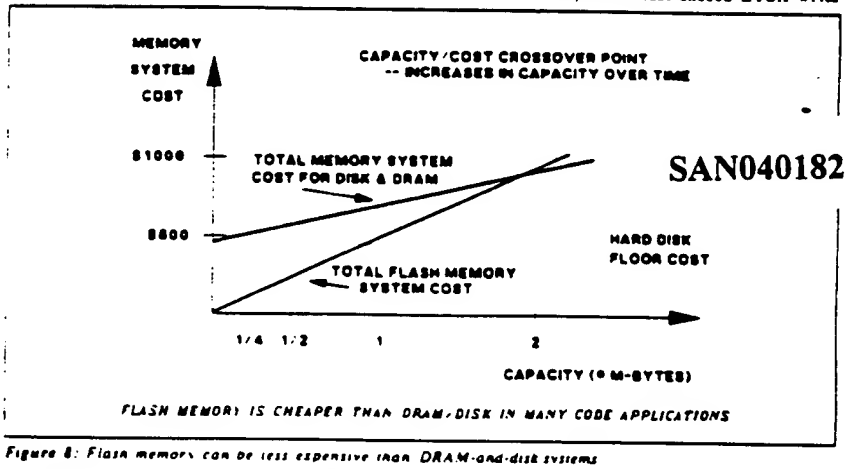

Figure 8: Flash memory can be less expensive than DRAM-and-disk systems

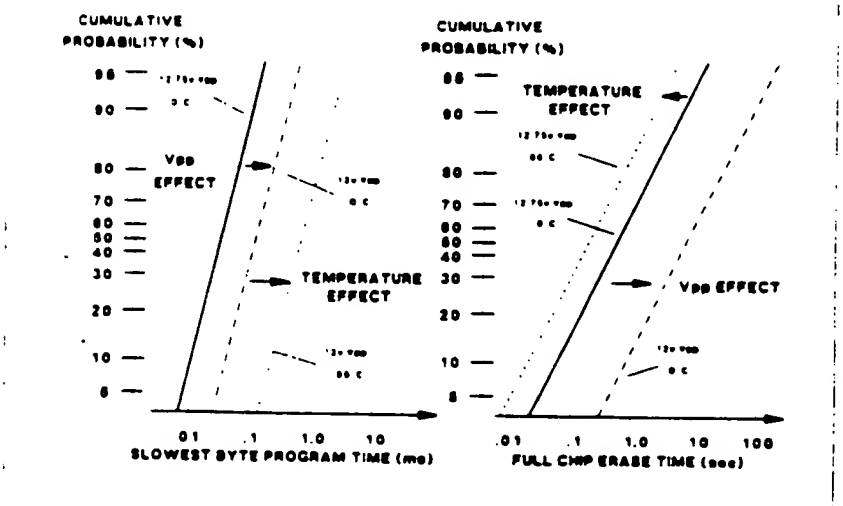

Figure 6: Temperature and programming voltage affect reprogramming rates. Intel offers EPROM-compatible 12.75-V programming flash memories which ensure successful reprogramming beyond the 10,000-cycle minimum endurance

endurance. Again, this is more a perception than reality. The most prolific PC user might store several letters, a couple large documents, a few spreadsheets, and dozens of graphics files in a given week. Including five-minute backup intervals, this barely reaches 2 Mbyte stored per week. Even with fairly inefficient "cycle management" (i.e., spreading cycling uniformly among all the flash devices), a 10-Mbyte flash-memory array would see less than 500 write cycles in 20 years. And since flash memories are directly, randomly accessible, the user sees instant response (instant writes, too, since writes can be handled as background tasks during subsequent file reads).

The bottom line is that computers read much more frequently than they write. This exactly matches the asymmetrical read/write performance of flash memory.

ETOX flash memory enables designers to create systems which are significantly more reliable, lighter, and faster than those based on other technologies. This could create a demand which far exceeds that for earlier nonvolatile memories. That, in turn, would drive volumes which might lever its small cell size into the lowest-cost alternative, and even the greatest skeptic would find low cost hard to ignore.

For more information on ETOX memory, contact Intel Corp., Literature Dept., P.O. Box 58065, Santa Clara, CA 95052-8065, (800) 548-4725.

SILICON BITS

Stan Baker

The Memory Driver

The primary driving force behind the personal computer revolution has been memory, not microprocessors. While one cannot give all the credit in one place, and microprocessors and software have their essential roles, the architectures and viability of these small computers has been due mostly to memory technologies—both semiconductor and magnetic.

That situation continues and more memory trends are afoot that will force computer systems in new directions in the near future. DRAMs are running out of the economic gas that has propelled the memory costs downward, not only leaving the door open for other memory technologies but demanding they enter.

Today's memory technologies are bubbling with new possibilities that will further revolutionize systems. At the heart of the changes will be nonvolatile devices. And the major player there will be flash technology.

The initial personal computers could have been made with CPU's that were not fully integrated, using gate arrays, LSI discrete logic or 2901 bit-slice architectures. But they could not have been made without low-cost, dense DRAM chips and low-cost floppy disk drives. The success of PCs then gave the economic stimulus to miniaturize hard disks which stimulated the PC business further.

The center of the computing universe is the data, not the processing engine. And the data is in the memory. And the ideal memory is nonvolatile.

Besides changing systems, the nonvolatile technologies will also alter the architecture of the semiconductor business internationally, with large scale impact on trade, political, and macro-economic issues. The leaders in the nonvolatile technologies are American companies. And they will not license their technology so readily as in the past.

There is a host of possibilities from flash, EPROM, EEPROM, battery backing, magnetic, optical, and the more remote ferroelectric technologies. Ferroelectric comes the closest to being the ideal nonvolatile RAM, but it is the furthest from reality. However, flash is here and, for the first time, promises to bring nonvolatile devices into the processing heart of computing systems in a big way.

Flash memories can have smaller cells than DRAMS and will be able to get more benefit from the latest lithographic and other processing equipment than DRAMs will. With only a year on the market the bit-count of flash devices has caught up with EPROMs and DRAMs, all now at 1 megabit per chip.

The 1-Mbit flash device just introduced by Intel has a die of 60,000 square mils. Current 1-Mbit DRAMs are larger, at about 70,000 square mils, and 256 kilobit SRAMs use about 75,000 square mils. 1-Mbit EEPROMs are about double, on the order of 130,000 square mils.

Flash will continue to track EPROM densities and soon outstrip even DRAMs, according to Richard Pashley, general manager of Intel's nonvolatile memory business. The only memory technologies that continue to track lithography in their cell size are EPROMs and flash devices.

Flash devices can be read as rapidly as EPROMs or DRAMs. But writing into them takes tens of microseconds per byte. And they are bulk erased in tens to hundreds of milliseconds.

Such long erase and write times may seem extremely limiting at first thought. But actually, the bulk of program and data storage does not need fast erase/write. That is why magnetic storage is so important. And that is what has some flash memory marketeers so excited—especially at Intel, which is nowhere in the DRAM and SRAM businesses, but the world leader in EPROMs. For flash devices are very similar to EPROMs.

Consider this example. If a computer were constructed with megabytes of fast volatile RAM directly serving the CPU, that can be erased and rewritten rapidly, massive blocks of nonvolatile flash RAM can take the place of magnetic storage backing that volatile memory. A few 4-Mbit flash chips will carry more data than most floppy disks.

That backup storage will significantly speed-up system performance and eliminate electro-mechanical reliability problems, as well as lots of weight and power drain. The flash devices can also be used to reduce the amount of volatile RAM, because some is used to store programs and data that seldom needs to be erased and changed. Such write-seldom sections of memory can be updated in a second or so, which is less than would irritate a human operator.

Fitting in this scenario, future microprocessors will have more and more memory on their die. That will be a good place for the fast RAM, made even faster by eliminating the inter-package wiring. And these internal RAMs will be organized to match the processing characteristics of the CPU which is not the case now with discrete RAMs. The flash and EPROM devices can then connect directly to the microprocessor package, eliminating discrete DRAMs and SRAMs.

Memory companies everywhere are working on flash devices. But Seeq Technology and Intel were the first to market. Since then, Texas Instruments and Toshiba have introduced versions. But Intel seems to be the only one supplying in significant volume, and it's Intel that has put the most corporate commitment—money and talent—behind flash. At Intel, flash technology plays directly off its EPROM technology in which Intel is still the world leader.

A passion for flash

According to Pashley, "flash is the way Intel will get back in the read-write memory business." In Pashley, Intel and perhaps the industry has its flash champion, and the success of any new technology depends on having the capable individuals that have the faith and lead the charge.

Pashley was the pioneer of scaling, the technique of shrinking MOS devices that is fundamental to the evolution of more and more dense MOS ICs. His process at Intel was termed "HMOS."

At the recent ISSCC in New York Intel described its 1-Mbit flash memory chip. Seeq Technology and National Semiconductor, who are jointly working on flash devices, described a 1-Mbit as well. And Texas Instruments described its latest flash, a 256k device that uses only a single 5-V supply.

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Memory

In today's dizzying array of memory choices, the design engineer's job is to match memory characteristics to the application. Intel has pioneered many memory devices to suit a wide variety of applications. The first step to narrowing down your choice is to determine the type of memory you are designing—data store or program store. After this has been done, the next step is to prioritize the following factors: Performance, Power Consumption, Density and Cost.

Most of this handbook is devoted to techniques and information to help you design and implement semiconductor memory in your application or system. Informative data sheets on DRAMs, SRAMs, EPROMs and Flash Memories contain many comprehensive charts, block diagrams, operating characteristics and programming modes. Application notes provide diagrams and hardware design information. In addition, there are many interesting and helpful article reprints.

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